Use of Supercapacitors to Improve Performance of GPRS Mobile Stations

CAP-XX Pty Ltd White Paper

February 2003

CAP-XX White Papers are produced as a means of providing product designers with useful information about CAP-XX supercapacitors and their applications. They are revised periodically to include new information. For detailed specifications of CAP-XX products, the reader is referred to the data sheet of the relevant product, which is available on request.

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Contents

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1. Introduction

CAP-XX supercapacitors combine the advantages of very high energy storage (typically 0.1F-1F) with very low Equivalent Series Resistance (ESR, typically 20mΩ - 100mΩ) enabling very high power delivery. This enables supercapacitors to supply relatively long peak loads (such as a GPRS class 10 or 12 transmit burst) for their entire duration.

Supercapacitors typically have much lower ESR (Equivalent Series Resistance) than a battery's output impedance. This means that a supercapacitor can supply a high current load and not suffer a large *I.R* drop at its output. Also, supercapacitors can be sized to have enough capacitance to provide the peak load for its duration without suffering too much voltage decay. With this combination, the load will see a much reduced voltage droop when drawing peak current than it otherwise would without the supercapacitor. This enables the application to extract more energy from the battery before reaching the minimum voltage level, thus increasing battery run time. Another way of thinking of this is that the supercapacitor averages the load as seen by the battery or voltage source.

Another application for supercapacitors is where the average load is less than the average power that a voltage source can deliver but peak load exceeds the peak power that can be delivered. Good examples of this are GPRS PC Cards with a 1A current limitation which draw 2A peak current. At 25% duty cycle (GPRS class 10), the average current is just approx 0.6A (0.1A drawn between peaks), and a supercap makes this possible. Similar situations apply with CF+ Cards which have a 0.5A limitation. The supercapacitor, with its very large energy storage and high power delivery acts as a filter to level the load, drawing average power from the source and delivering peak power to the load.

2. Problem Outline

GPRS transmission typically requires a peak current of 2A from the voltage supply during transmission burst. For GSM and GPRS class 2 or class 8, the transmit burst is only 577μsecs long, so supplying the necessary power for the duration of transmission was manageable using traditional tantalum capacitors. However, with GPRS class 10 (1.15msecs transmit burst duration) and GPRS class 12 (2.3msecs transmit burst duration), traditional capacitors do not have sufficient energy storage to provide adequate voltage support for the battery during transmission.

For a battery powered unit, this means that the battery needs to provide the full peak current during transmission and suffers a voltage droop = peak current x battery pack output impedance. Typically this is 2A x 250mΩ = 0.5V. The result is that the circuit suffers from a low voltage shutdown while there is still plenty of energy left in the battery. This means the battery run time is much shorter than it otherwise would be.

At low temperatures (<0°C) the battery pack output impedance is considerably greater. This exacerbates the problem described above and results in unacceptably short run times in cold temperatures.

For a PC Card, where the peak current drawn is specified as < 1A[1], or a CF+ card, where the peak current is specified as < 0.5A, GPRS transmission is not possible without energy storage and load leveling on the card. This can be done in one of two ways:

- Incorporate a small battery and associated battery charging and protection circuit in the PC Card/CF+ Card module, charged from the PC card/CF+ Card bus to provide the 2A peak current during transmission
- Use a supercapacitor to provide pulse power and average the load seen by the host PDA or notebook computer.

3. Characteristics of Supercapacitors

Physical Construction

A traditional capacitor stores energy in the electric field created by charge separation. The electric field normally exists in a dielectric which becomes polarised. The capacitance is proportional to the permittivity of the dielectric and the area of the plates and inversely proportional to the separation distance of the plates.

There is no intervening dielectric material in a supercapacitor. Fig 1 shows the typical construction for one layer of a CAP-XX supercapacitor.

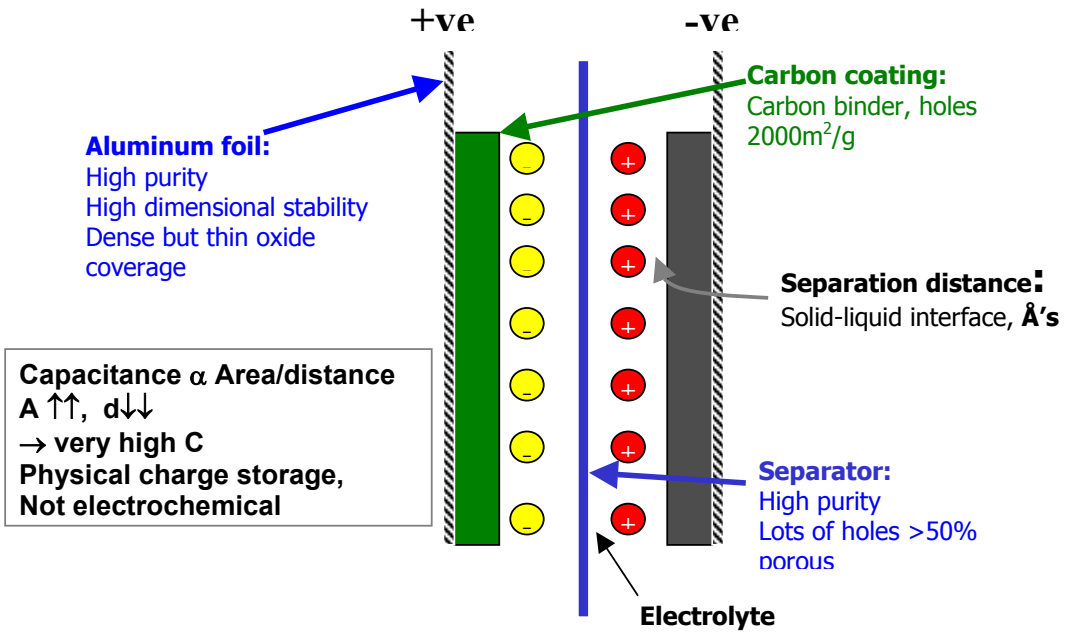


Fig 1 What's inside a Supercapacitor?

[1] The peak = 3.3W, specified as either 1A @ 3.3V or 660mA @5V.

The physical construction is similar to that of a battery with two electrodes immersed in an electrolyte with a separator between them. However, unlike a battery there is no chemical energy storage. There are effectively two capacitors in series within each supercapacitor. Each has a set of plates consisting of a carbon electrode and an adjacent electrolyte containing ions. Charges are not bound in the electrolyte. They are free to move anywhere within the electrolyte which also penetrates the pores of the carbon electrodes. The separator insulates the two electrodes whilst allowing the ions to pass through it.

Each electrode pair, as shown in Fig 1, is made from aluminium current collectors coated by activated carbon and separated by a porous membrane. The carbon coating has many holes in its structure which achieves a very high surface area for the electrodes, up to 2000m^2 per gram. Passage of ions in the electrolyte through the porous membrane is how charge is transferred in the device. Ions enter the pores in the carbon and place themselves against the surface of the activated carbon electrode which contains ions of the opposite polarity. This is the charge storage mechanism. The separation distance between the ions is approximately their molecular width.

This results in a capacitor with a charge storage area in the order of 000's m^2 and a charge separation in distance in the order of Å. Since capacitance is proportional to charge storage area / charge separation distance, we have a capacitor with a small form factor (approx the size of a postage stamp and 2mm – 3mm thick) and a huge C (0.1F – 1.4F @ 4.5V), hence "Supercapacitor".

CAP-XX devices come in two standard form factors: 28.5mm x 17mm and 39mm x 17mm. We vary the C & ESR by varying the number of layers, coating thickness and carbon composition. Appendix A is a set of CAP-XX product bulletins with the available devices.

Electrical Characteristics

The capacitance of a supercapacitor is a function of voltage, current, frequency, temperature and time.

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain it can be found by applying a step discharge current to a charged capacitor as in Fig 2. In this example the supercapacitor is pre-charged and then discharged with a current pulse (I). The ESR is found by dividing the instantaneous voltage step (ΔV) by I. The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage and multiplying it by I. The effective capacitance (C_e) is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. C_e shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

CAP-XX uses this pulse discharge method for characterizing their devices.

As there is no dielectric in a supercapacitor, the breakdown voltage is governed by the chemistry at the electrolyte-carbon interface. A single supercapacitor cell with an organic electrolyte is limited to an operating voltage = 2.3V. CAP-XX produces single cell devices and dual cell devices rated at 4.5V suitable for operation with a LiIon battery.

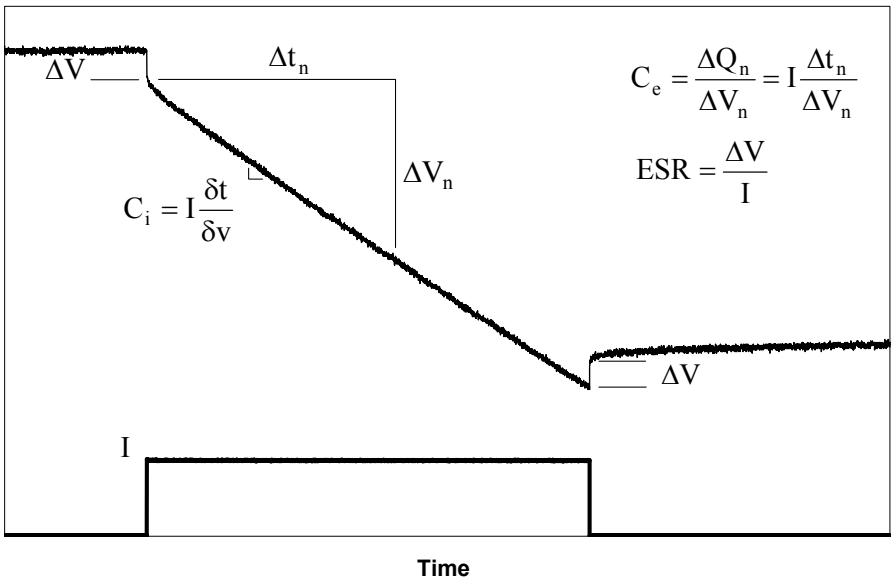


Fig 2 Definitions for effective capacitance, instantaneous capacitance and ESR

Supercapacitors exhibit distributed capacitance. This is due to the time it takes ions in the electrolyte to migrate in and out of the pores in the electrolyte. The ions at the mouth of the pores are available very quickly while those deeper in take a longer time to make their charge available. A good model of a supercapacitor is an RC ladder network.

This means care is required when interpreting electrical measurements on supercapacitors. When measuring frequency response on an RLC bridge with a sine wave, capacitance appears to roll off in the 10-100Hz range. However, when looking at supercapacitor pulse response in the time domain, it appears there is sufficient effective capacitance at the leading edge to support a 1.15msec pulse for GPRS transmission, see Fig 3a and Fig 3c below. This implies a frequency response > 9Khz (3rd odd harmonic for a 1KHz square wave).

The series of figures 3a, 3b and 3c demonstrates the supercapacitor's high energy storage and high power delivery using the example of a GPRS class 10 pulse drawing 2A from a 600mAh LiIon battery. It also shows that the supercapacitor's frequency response is also more than sufficient for the task.

Fig 3a shows a 2A pulse drawn from a LiIon battery with no capacitor providing voltage support. There is a voltage droop at the battery's output of

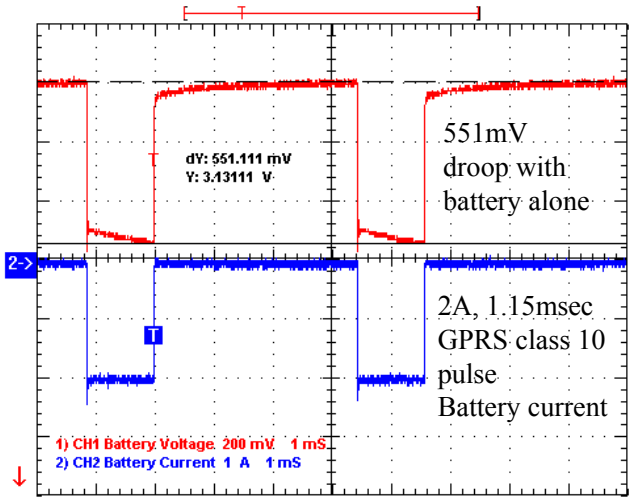


Fig 3a, Battery with no capacitors

550mV which is ≈ 2A x 250mΩ (output impedance of the battery pack). There is an additional voltage droop during the pulse as the battery discharges.

Fig 3b shows the effect of 8 x 470µF tantalum capacitors in parallel. Even though the combined ESR is very low (≈ 7mΩ), the ≈4mF capacitance has insufficient energy storage to sustain the 2A load for its duration. The capacitors suffer considerable voltage decay so that the peak battery current ≈ 1.5A, and the voltage droop has been reduced only by 160mV from the no capacitor case shown in Fig 3a.

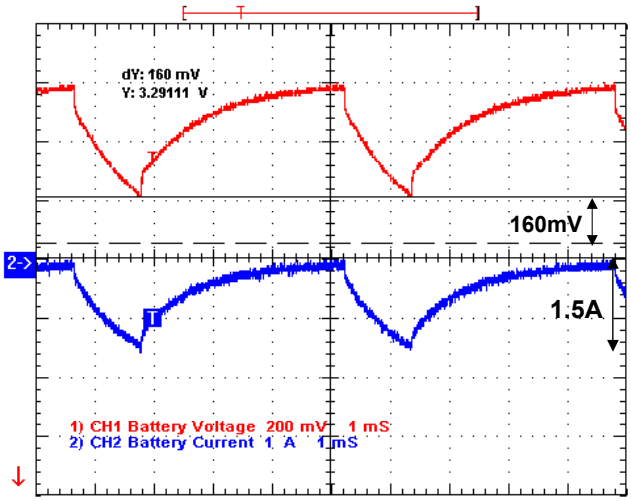


Fig 3b, battery + 8 x 470uF caps

Fig 3c shows the voltage support provided by a CAP-XX supercapacitor rated at 0.3F and 60mΩ ESR. The voltage ripple is 120mV (=2A x 60mΩ), and the capacitance is so high that there is no appreciable voltage decay during the pulse. Also note that the supercapacitor's frequency response has been good enough to result in a square pulse.

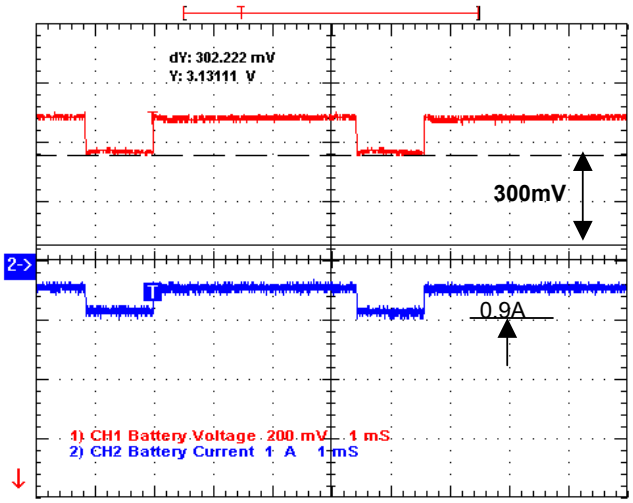


Fig 3c, battery + supercapacitor, 0.3F

4. Extension of battery Run Time and Low Temperature Operation

Circuits with pulsed peak power requirements, such as GPRS mobile stations, usually stop operating when the minimum voltage threshold is crossed as a result of the voltage droop during transmission. There is often plenty of energy left in the battery when this occurs. Our experiments show there can be up to 50% energy remaining when the unit shuts down, as shown in Figs 4 & 5 below.

Fig 4 shows the battery run time for a minimum threshold of 3.3V with and without supercapacitor. Without the supercapacitor the battery suffers a 0.5V droop during the 2A pulse and the battery crosses the minimum 3.3V threshold after 15 mins continuous transmission. With the supercapacitor, the voltage droop is only 150mV and the 3.3V threshold is breached after 36 mins resulting in a 140% improvement.

Note that the average voltages without and with supercapacitor (Vavn25P1, Vavw25P1 respectively in Fig 4) are the same. This is as expected since the supercapacitor simply averages the load. However, this must be considered in any

battery low-voltage detection algorithm, since any algorithm based on the average battery voltage, or the unloaded battery voltage, will not exploit this improved performance unless it is modified to account for the reduced voltage droop under load.

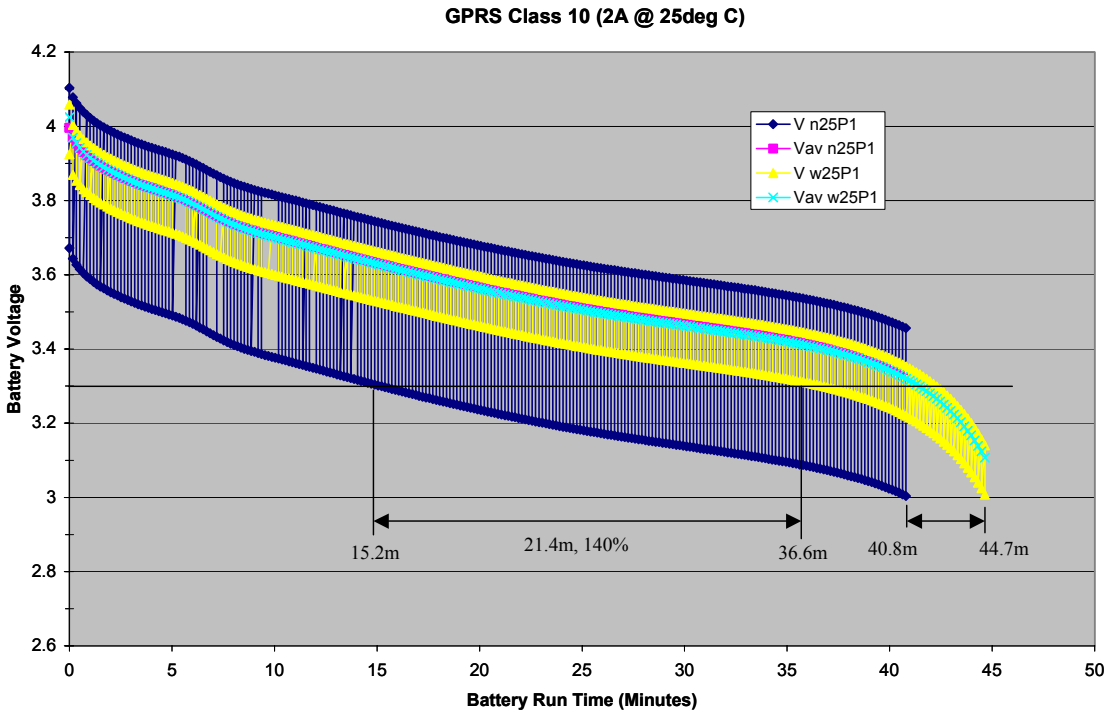


Fig 4, 600mAh Battery run time extension with supercapacitor, 3.3V cutoff

Fig 5 shows the % increase in battery run time for a minimum threshold voltage of 3.3V as a function of battery cycles at 25°C. This result is the average of tests on five 600mAh LiIon batteries. As batteries age, their output impedance increases, thereby increasing the benefit gained from using a supercapacitor. The run time extension for continuous transmission increases from approx 90% to 160%. This equates to extracting an extra 45% to 60% of the energy available in the battery.

Fig 6 shows the minutes run time at 0°C without supercapacitor and the extra run time with supercapacitor, averaged over five 600mAh LiIon batteries. This graph highlights the very short run time without supercapacitor and the significant improvement with supercapacitor.

Refer to Appendix B, CAP-XX Application Brief 1004, for further discussion on battery run time extension and low temperature boost.

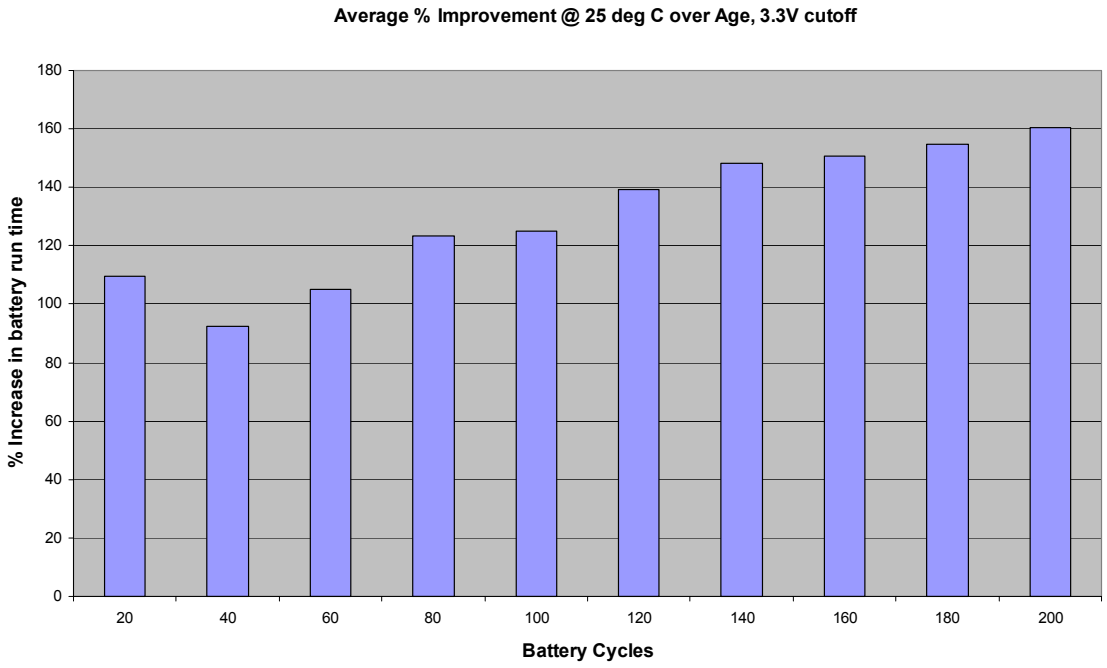


Fig 5, % battery runtime improvement with supercapacitor, 3.3V cutoff

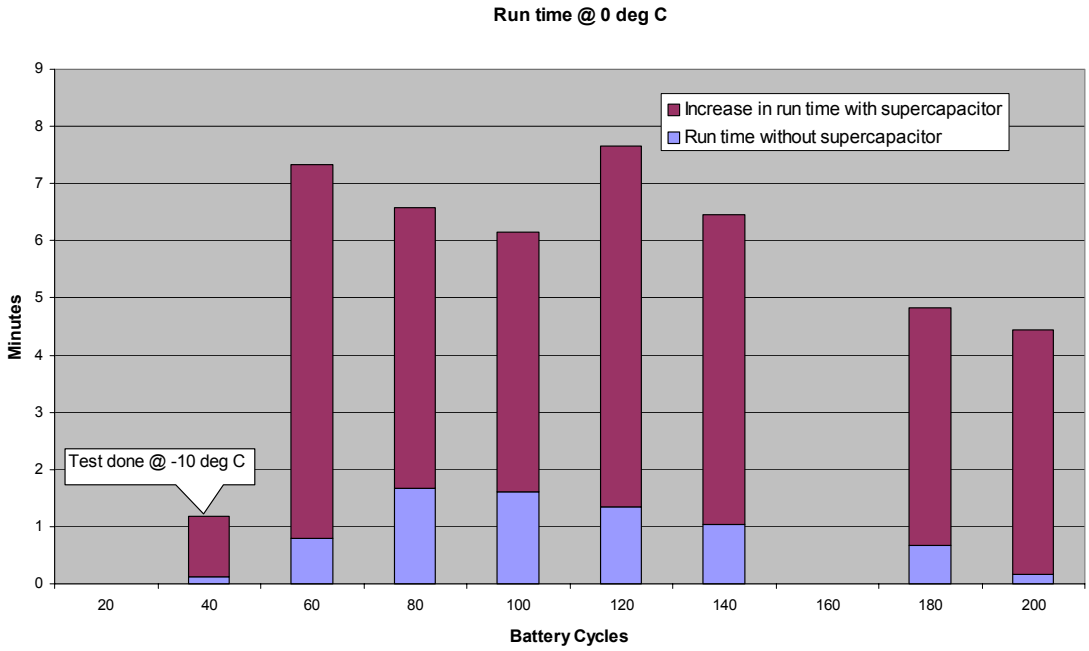


Fig 6, Battery runtime increase @ 0°C with supercapactor

5. Compact Flash and PC Card Applications

In this application, the supercapacitor averages the load seen by the source.

The PC Card specification limits the peak current drawn by the card to 1A, while most GPRS transmitters require 1.5A-2A to transmit at full power for a pulse duration of 1.154msecs with a duty cycle of 25% for class 10 operation, and for a pulse duration of 2.308msecs with a duty cycle of 50% for class 12 operation. This is not possible without some means of averaging the load power.

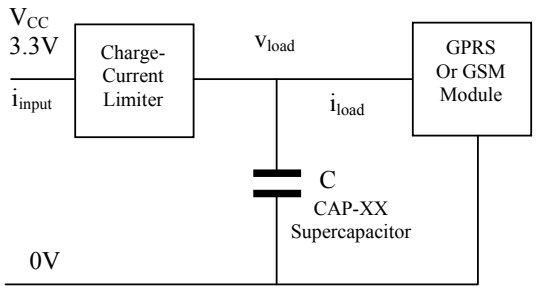


Fig 7 shows the block diagram for supplying power to a PC or CF+ card with a supercapacitor.

If the load draws a steady state current I_{steady}, and a peak current I_{peak} with a duty cycle D, then the average current drawn from the supply:

$$I_{average} = I_{steady} + D \cdot I_{peak}$$

Fig 7, Block diagram for GPRS power

For a solution to be viable, I_{averag} < max current specification. By way of example if I_{steady} = 0.05A, I_{peak} = 1.6A, D = 25% (GPRS class 10), then

$$I_{average} = 0.05A + 0.25 \times 1.6A = 0.45A$$

For this example, a solution for PC cards (max current < 1A) is easily attainable, and a solution for CF+ cards (max current < 0.5A) is possible in principle, but requires more detailed analysis to ensure that the 0.5A maximum current is adhered to after losses are accounted for.

CAP-XX has developed a spreadsheet simulation tool to calculate current and voltage profiles for a given steady state and pulsed load, supercapacitor C and ESR, and source voltage and impedance.

Fig 8 below shows how a supercapacitor averages a 2A GPRS class 10 load to meet the PC Card maximum current constraint. The source was 3.3V, 200mΩ output impedance. The load was 100mA continuous current + 1.9A pulse current for 1.154ms every 4.616ms.

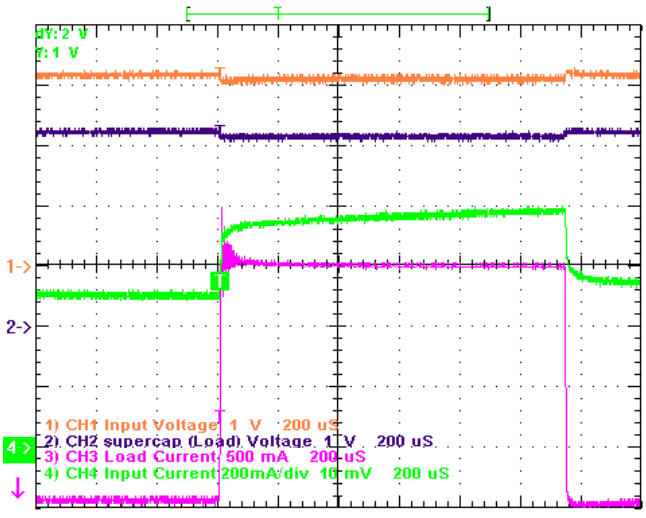


Fig 8, Load averaging with a supercapacitor, PC card, GPRS class 10

The top two traces show voltage at the source and the load (1V/div). The voltage droop with the supercapacitor is negligible. The bottom trace shows load current with a 2A peak while the 3rd trace shows the load seen by the supply, averaged by the supercapacitor, with an 800mA peak and 300mA p-p ripple.

Appendix C contains Application Briefs 1009, 1010, 1011 which describe PC card applications for GPRS class 10 & 12, and CF+ card class 8. These application briefs contain tables of supercapacitors suitable for these applications.

Appendix D contains Application Note 1003, which describes in detail the equations governing the selection of the appropriate supercapacitor, and the use of the spreadsheet simulation tool which is based on those equations.

6. Circuit Considerations

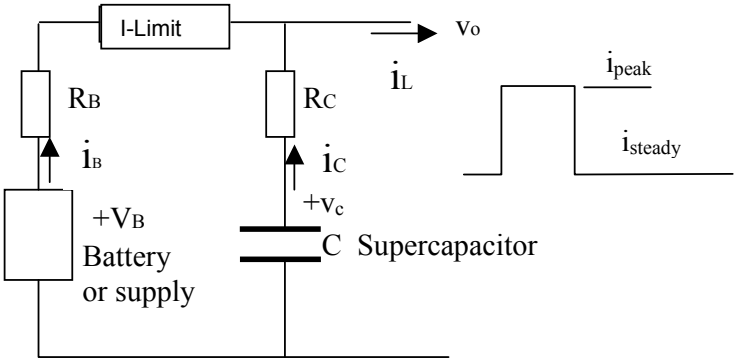


Fig 9, generic power circuit with supercapacitor

Inrush Current:

Supercapacitors, with their very large C and very low ESR would attempt to draw inrush currents at power up that would cause a battery protection circuit or PC Card/CF Card supply to shutdown. Consider the following example, referring to Fig 9:

Source impedance, $R_B = 200m\Omega$

Supercap ESR, $R_C = 100m\Omega$

Supercap C = 0.3F

Supply voltage, $V_B = 3.6V$

At t=0, with discharged supercapacitor, with no current limit,

$I_{inrush} = V_B/(R_B + R_C) = 3.6V/(200m\Omega + 100\ m\Omega) = 12A$

At one RC time constant later (0.03s), the current would still be approx 4A

The inrush current limit circuit can be either a one time limit (limits charge current at power up, but once the supercap is charged the MOSFET that performs the limiting function remains hard on until power off), or a dynamic current limit that is always active.

Appendix E contains Application Note 1002 Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices.

Dynamic Current Limit:

Referring to Fig 9, and making the 1st order assumption that the voltage decay at the supercap is negligible during the peak load, and the supercap voltage, $v_c \approx$ source voltage, V_B then:

$$i_B / i_C \approx R_C / R_B$$

This means that the source current can be limited to the desired value by reducing the supercapacitor ESR. However, if this requires an ESR value that is too low, for example, size constraints on the supercapacitor make the desired ESR impractical, then a dynamic current limiter may be used limit the source current to the desired value. This dynamic current limiter also serves to limit inrush current.

If a dynamic current limiter is used, then you need to check that the voltage at the load remains above the minimum required. The CAP-XX supercap spreadsheet simulation tool caters for dynamic current limiting.

Circuit #3 in Application Note 1002 is a dynamic current limit circuit.

7. Environmental

The following environmental tests have been conducted:

Operating Temperature

CAP-XX has two families of devices with the following operating temperatures:

- -30°C to +75°C
- -30°C to +85°C

Figs 10 & 11 show the variation of capacitance and ESR with temperature for the two families of supercapacitors. Note that capacitance is invariant with temperature. ESR increases at low temperatures due to the reduced conductivity of the electrolyte.

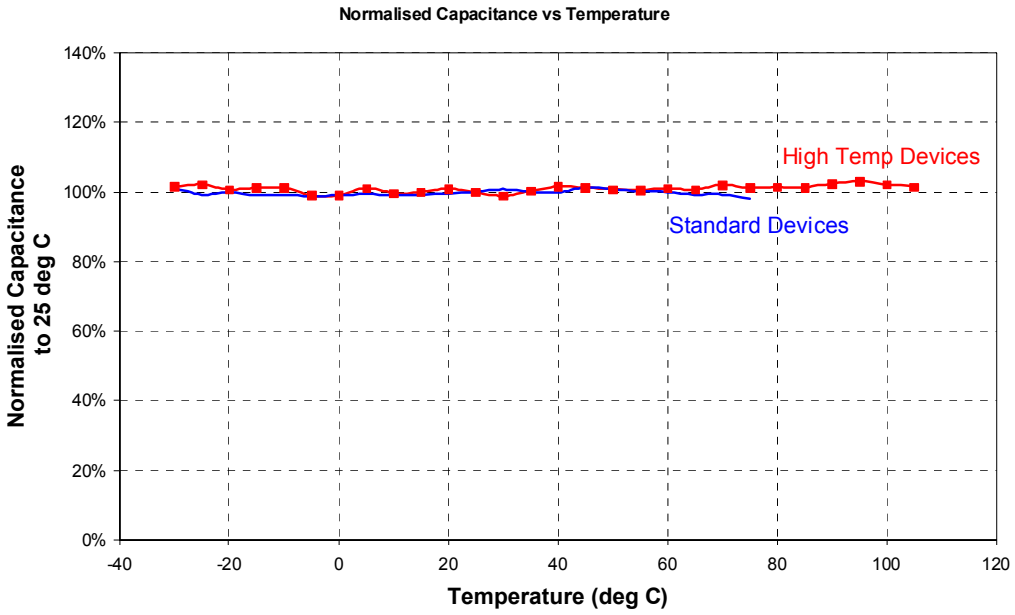


Fig 10, Capacitance change with temperature

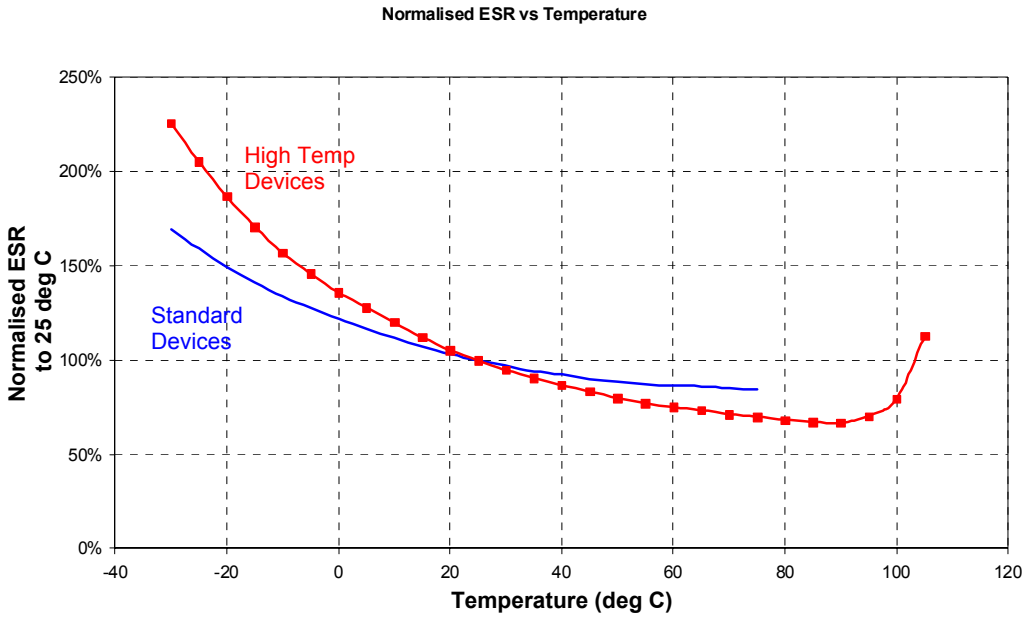


Fig 11, ESR change with temperature

Vibration

Tested to IEC68-2-6

Type	Sinusoidal
Frequency	55Hz-500Hz
Amplitude	0.35mm±3dB (55Hz to 59.55Hz) 5g±3dB (59.55Hz to 500Hz)
Sweep Rate	1 Oct/min
No. of Cycles	10 (55Hz-500Hz-50Hz)
No. of Axis	3 orthogonal
Results	No electrical or mechanical degradation (adhesive not required)

Shock

Tested to IEC68-2-27

Pulse Shape	Half Sine
Amplitude	30g±20%
Duration	18ms±5%
No. of Shocks	3 in each direction (18 in total)
No. of Axis	3 orthogonal
Results	No electrical or mechanical degradation (adhesive not required)

Drop Test

Tests performed	Three drops of test jig, each axis from 6 feet onto concrete.
Results	No electrical or mechanical degradation when following the mounting rules.

Mounting

Unconstrained	If the supercapacitor is unconstrained then some form of adhesive should be used to affix the supercapacitor to the PCB.
Constrained	If the supercapacitor is constrained with a maximum clearance of 1mm then the adhesive is not required.

Soldering

The recommended maximum soldering time is 5 seconds when using an iron at 400°C in an ambient temperature of 25°C.

8. Safety

CAP-XX supercapacitors are constructed from inert materials: carbon, aluminium, organic electrolyte. The volume of electrolyte in a supercapacitor is << 1ml and is absorbed in the carbon, so if a device was cut open there would be no leaking of liquid electrolyte.

The device is not inherently polarised when constructed. Only after it has been held at voltage during production does the supercapacitor attain a preference for a positive and negative terminal when different ion species migrate to the +ve and –ve electrodes. However, if reverse bias voltage is applied to the device, the only consequence will be a slight increase in ESR. This is due to the forced migration of ions to the opposite electrode. There will be no fire, smoke or explosion.

Similarly, if over-voltage is applied to the device, the only consequence will be a slight swelling and a rise in ESR, eventually progressing to an open circuit. There will be no fire, smoke or explosion.

The failure mode for CAP-XX supercapacitors is high ESR.

The following tests have been conducted:

Puncture test:

Metal dart dropped onto a fully charged supercapacitor, puncturing the device.

Result: No smoke, no fire.

Pyrolysis test:

Supercapacitor incinerated in an oven heated to 800 deg C. Resulting compounds analysed.

Result: No toxic chemicals detected.

Appendix A

CAP-XX Product Bulletins

Product Bulletin
GW1 Series - Double Layer Supercapacitor

cap-XX

The GW1 series of CAP-XX supercapacitors are low profile, low impedance (low ESR) power sources that are designed to overcome both the power delivery limitations of battery systems and the energy delivery limitations of conventional capacitors.

The features of CAP-XX supercapacitors are:

- Provide high power for peak current loads (low ESR)
- Store sufficient energy to enable power surges (high capacitance)
- Operate at low (-30 ºC) temperature
- Smallest devices for given ESR and capacitance (high power and energy density)

CAP-XX Model Number	DC Capacitance ± 20%*	ESR ± 20%*	Height Maximum
GW 1 10A	650 mF	16 mΩ	2.28 mm
GW 1 11A	1600 mF	18 mΩ	2.46 mm
GW 1 08A	550 mF	20 mΩ	1.91 mm
GW 1 13A	2800 mF	28 mΩ	2.50 mm
GW 1 03A	950 mF	30 mΩ	1.58 mm
GW 1 02A	350 mF	30 mΩ	1.36 mm
GW 1 07A	800 mF	34 mΩ	1.36 mm
GW 1 01A	650 mF	40 mΩ	1.14 mm
GW 1 09A	250 mF	45 mΩ	0.99 mm
GW 1 04A	1600 mF	45 mΩ	1.54 mm
GW 1 05A	500 mF	55 mΩ	0.92 mm
GW 1 14A	180 mF	60 mΩ	0.81 mm
GW 1 12A	400 mF	185 mΩ	0.70 mm

GW1 Parameter	Minimum	Nominal	Maximum
Operating Temp	-30°C	+20°C	+75°C
Storage Temp	-40°C		+75°C
Voltage		2.25V	2.5V (peak)
Length	27.5mm	28.5mm	29.0mm
Width	16.5mm	17.0mm	17.5mm
ESR change with Temp	75% of nominal @ +75°C		150% of nominal @ -20°C
Pulse Current	-	-	30A

* Tolerance is based on nominal operating temperature, +20°C

Reduced voltage drops – Reduce DC/DC requirements

Solve RF power limitations in wireless PDAs, smart phones

Enable fuel cells and alkaline batteries to replace Li ion

Extend battery life of Digital Cameras

Extend low temperature (-30ºC) operation of wireless devices

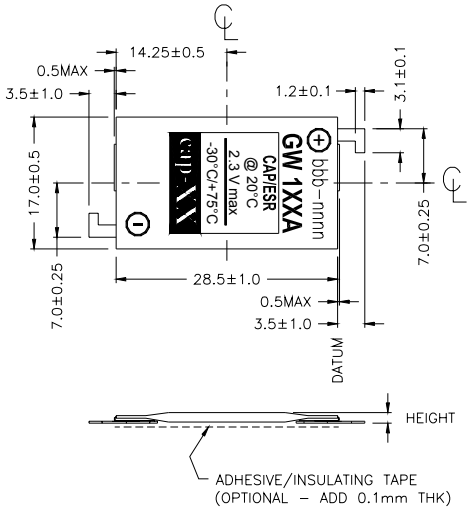
Solve current limitations in PCMCIA and CF cards

Eliminate power loss from battery chatter

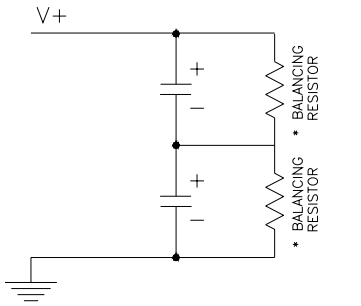
Further Information:

CAP-XX also offers other packaging options and temperature ranges. Additional product information and application resources can be obtained from CAP-XX by using the contact details below or on our web site at www.CAP-XX.com. CAP-XX will gladly discuss specific requirements, and our Applications Engineers will work together with a client to develop a solution that meets your needs.

Mechanical Drawings

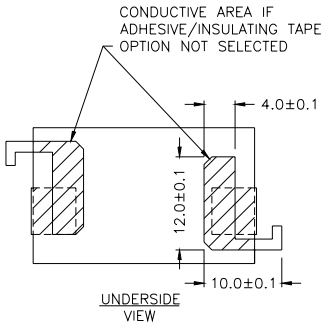


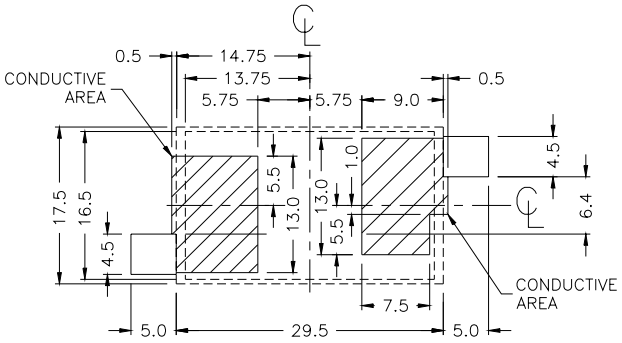
Electrical Drawing



* REFER TO cap-XX APPLICATION TEAM FOR VALUES

SUGGESTED CONNECTION DETAILS USING 2 GW 1XX SUPERCAPS IN SERIES





SUGGESTED PAD LAYOUT

PAD LAYOUT ONLY CATERS FOR cap-XX MANUFACTURING TOLERANCES. THE CUSTOMER MUST INCREASE PAD SIZE TO ALLOW FOR ANY PLACEMENT TOLERANCES.

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sales@CAP-XX.com
www.CAP-XX.com

Product Bulletin

GW2 Series - Double Layer Supercapacitor

cap-XX

The GW2 series of CAP-XX supercapacitors are low profile, low impedance (low ESR) power sources that are designed to overcome both the power delivery limitations of battery systems and the energy delivery limitations of conventional capacitors.

The features of CAP-XX supercapacitors are:

- Provide high power for peak current loads (low ESR)
- Store sufficient energy to enable power surges (high capacitance)
- Operate at low (-30 ºC) temperature
- Smallest devices for given ESR and capacitance (high power and energy density)

CAP-XX Model Number	DC Capacitance ± 20%*	ESR ± 20%*	Height Maximum
GW 2 10D	350 mF	32 mΩ	4.63 mm
GW 2 11D	800 mF	34 mΩ	4.99 mm
GW 2 08D	300 mF	40 mΩ	3.90 mm
GW 2 13D	1400 mF	55 mΩ	5.07 mm
GW 2 03D	500 mF	55 mΩ	3.23 mm
GW 2 02D	180 mF	60 mΩ	2.79 mm
GW 2 07D	400 mF	65 mΩ	2.79 mm
GW 2 01D	300 mF	85 mΩ	2.35 mm
GW 2 09D	120 mF	90 mΩ	2.06 mm
GW 2 04D	800 mF	95 mΩ	3.15 mm
GW 2 05D	250 mF	110 mΩ	1.91 mm
GW 2 14D	90 mF	115 mΩ	1.69 mm

GW2 Parameter	Minimum	Nominal	Maximum
Operating Temp	-30°C	+20°C	+75°C
Storage Temp	-40°C		+75°C
Voltage		4.5V	5.0V (peak)
Length	27.5mm	28.5mm	29.5 mm
Width	16.5mm	17.0mm	17.5mm
ESR change with Temp	75% of nominal @ +75°C		150% of nominal @ -20°C
Pulse Current	-	-	30A

* Tolerance is based on nominal operating temperature, +20°C

Reduced voltage drops – Reduce DC/DC requirements

Solve RF power limitations in wireless PDAs, smart phones

Enable fuel cells and alkaline batteries to replace Li ion

Extend battery life of Digital Cameras

Extend low temperature (-30ºC) operation of wireless devices

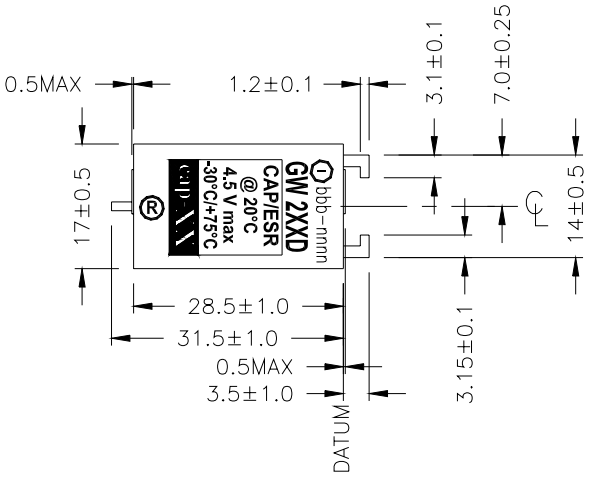
Solve current limitations in PCMCIA and CF cards

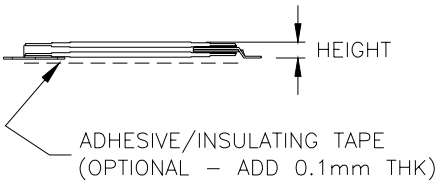
Eliminate power loss from battery chatter

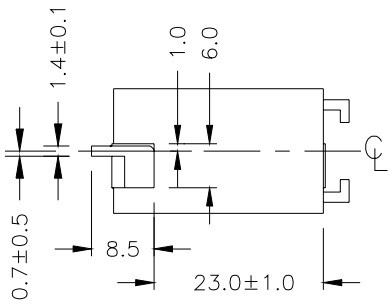
Further Information:

CAP-XX also offers other packaging options and temperature ranges. Additional product information and application resources can be obtained from CAP-XX by using the contact details below or on our web site at www.CAP-XX.com. CAP-XX will gladly discuss specific requirements, and our Applications Engineers will work together with a client to develop a solution that meets your needs.

Mechanical Drawings

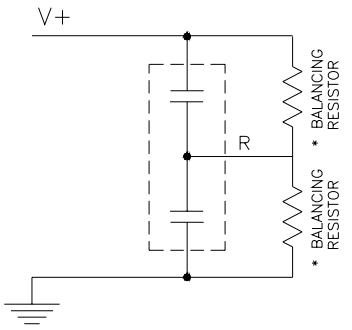






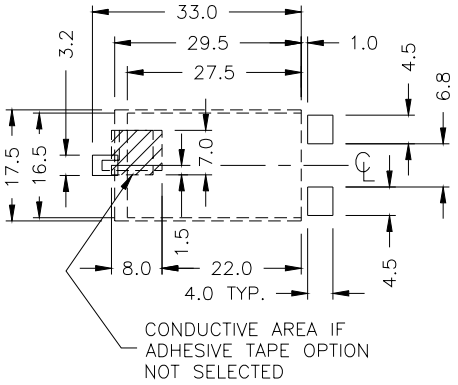
UNDERSIDE VIEW

Electrical Drawing



* REFER TO cap-XX APPLICATION TEAM FOR VALUES

SUGGESTED CONNECTION DETAILS FOR GW 2XX SERIES SUPERCAP



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Product Bulletin
GS1 Series - Double Layer Supercapacitor

cap-XX

The GS1 series of CAP-XX supercapacitors are low profile, low impedance (low ESR) power sources that are designed to overcome both the power delivery limitations of battery systems and the energy delivery limitations of conventional capacitors.

The features of CAP-XX supercapacitors are:

- Provide high power for peak current loads (low ESR)
- Store sufficient energy to enable power surges (high capacitance)
- Operate at low (-30 ºC) temperature
- Smallest devices for given ESR and capacitance (high power and energy density)

CAP-XX Model Number	DC Capacitance ± 20%*	ESR ± 20%*	Height Maximum
GS 1 08A	2700 mF	10 mΩ	2.46 mm
GS 1 05A	950 mF	12 mΩ	1.91 mm
GS 1 07A	1900 mF	14 mΩ	1.80 mm
GS 1 10A	4900 mF	16 mΩ	2.50 mm
GS 1 11A	650 mF	18 mΩ	1.36 mm
GS 1 04A	550 mF	22 mΩ	1.18 mm
GS 1 03A	400 mF	26 mΩ	0.99 mm
GS 1 06A	1100 mF	26 mΩ	1.14 mm
GS 1 01A	2800 mF	28 mΩ	1.54 mm
GS 1 02A	300 mF	34 mΩ	0.81 mm
GS 1 12A	200 mF	50 mΩ	0.74 mm
GS 1 09A	700 mF	110 mΩ	0.70 mm

GS1 Parameter	Minimum	Nominal	Maximum
Operating Temp	-30°C	+20°C	+75°C
Storage Temp	-40°C		+75°C
Voltage		2.25V	2.5V (peak)
Length	38.0mm	39.0mm	40.0mm
Width	16.5mm	17.0mm	17.5mm
ESR change with Temp	75% of nominal @ +75°C		150% of nominal @ -20°C
Pulse Current	-	-	30A

* Tolerance is based on nominal operating temperature, +20°C

Reduced voltage drops – Reduce DC/DC requirements

Solve RF power limitations in wireless PDAs, smart phones

Enable fuel cells and alkaline batteries to replace Li ion

Extend battery life of Digital Cameras

Extend low temperature (-30ºC) operation of wireless devices

Solve current limitations in PCMCIA and CF cards

Eliminate power loss from battery chatter

Further Information:

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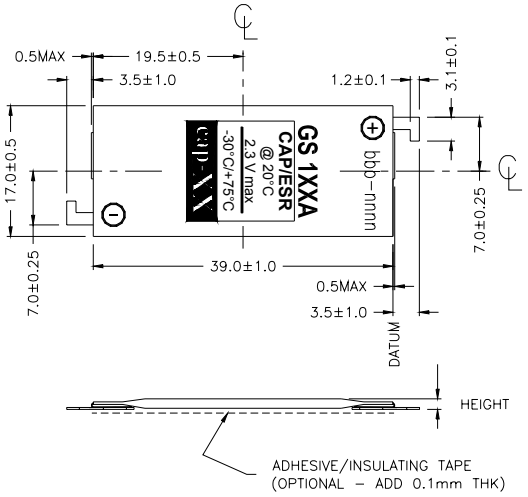
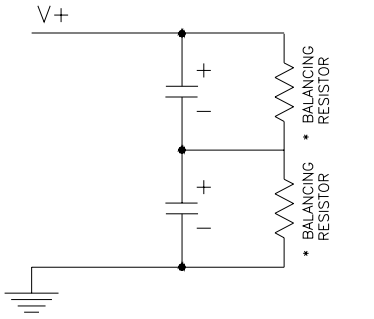
Mechanical Drawings



Electrical Drawing



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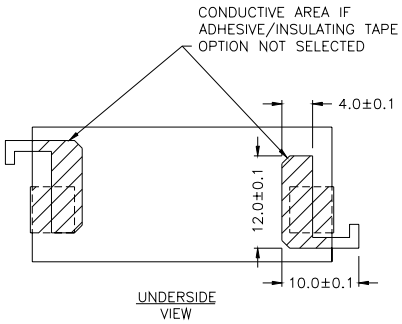
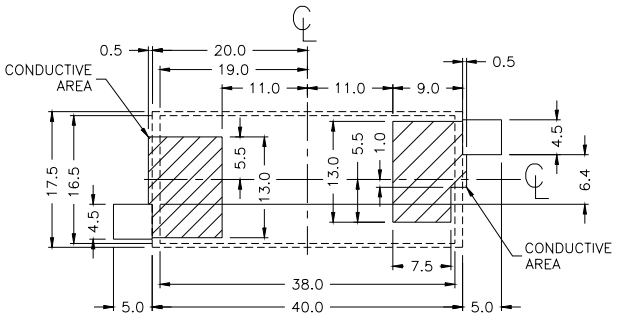
SUGGESTED CONNECTION DETAILS USING 2 GS 1XX SUPERCAPS IN SERIES





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Product Bulletin

GS2 Series - Double Layer Supercapacitor

cap-XX

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- Smallest devices for given ESR and capacitance (high power and energy density

CAP-XX Model Number	DC Capacitance ± 20%*	ESR ± 20%*	Height Maximum
GS 2 08D	1400 mF	20 mΩ	4.99 mm
GS 2 05D	450 mF	24 mΩ	3.90 mm
GS 2 07D	950 mF	28 mΩ	3.67 mm
GS 2 10D	2400 mF	32 mΩ	5.07 mm
GS 2 11D	300 mF	34 mΩ	2.79 mm
GS 2 04D	250 mF	40 mΩ	2.43 mm
GS 2 03D	200 mF	50 mΩ	2.06 mm
GS 2 06D	550 mF	50 mΩ	2.35 mm
GS 2 01D	1400 mF	55 mΩ	3.15 mm
GS 2 02D	160 mF	70 mΩ	1.69 mm
GS 2 12D	100 mF	100 mΩ	1.55 mm
GS 2 09D	350 mF	215 mΩ	1.47 mm

GS2 Parameter	Minimum	Nominal	Maximum
Operating Temp	-30°C	+20°C	+75°C
Storage Temp	-40°C		+75°C
Voltage		4.5V	5.0V (peak)
Length	38.0mm	39.0mm	40.0mm
Width	16.5mm	17.0mm	17.5mm
ESR change with Temp	75% of nominal @ +75°C		150% of nominal @ -20°C
Pulse Current	-	-	30A

* Tolerance is based on nominal operating temperature, +20°C

Reduced voltage drops – Reduce DC/DC requirements

Solve RF power limitations in wireless PDAs, smart phones

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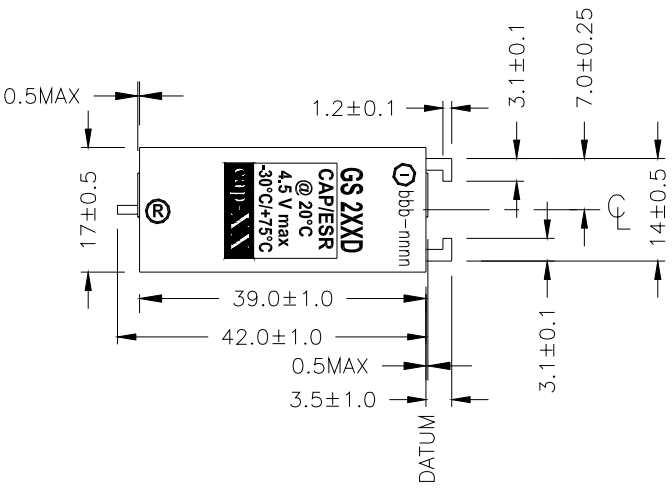
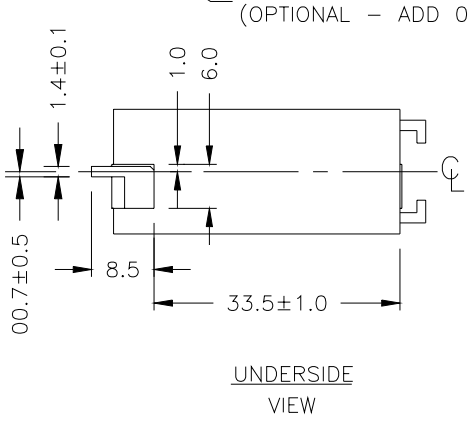
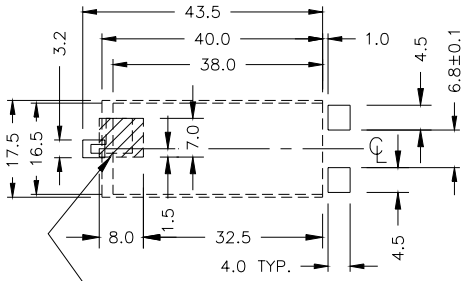




UNDERSIDE VIEW



SUGGESTED PAD LAYOUT

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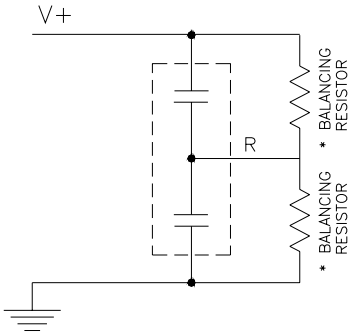
Electrical Drawing



* REFER TO cap-XX APPLICATION TEAM FOR VALUES

SUGGESTED CONNECTION DETAILS FOR GS 2XX SERIES SUPERCAP

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Appendix B

Application Brief No. 1004

Battery Run-Time Extension and Low-Temperature Boost

CAP-XX APPLICATION BRIEF No. 1004

Battery Run-Time Extension and Low-Temperature Boost

Version 2, August 2002

Outline

Pulsed loads occur in many battery-powered portable devices. These loads can cause enough voltage-drop to crash the device. At low temperatures (such as < 0°C), the situation can be still worse, as common batteries, like Lithium-ion and NiMH (Nickel-Metal Hydride), exhibit vastly reduced capacity and increased internal resistance. A **CAP-XX supercapacitor** used in a parallel hybrid combination with the battery can reduce the voltage excursions under load, permitting a device to operate reliably until most of the battery's energy has been used, or allowing it to function in cold conditions in which it normally fail or shut down after a short time. The supercapacitor also helps to protect the battery from potentially damaging voltage drops and current peaks, which may be of particular benefit to Lithium-ion batteries.

The Problem

- Pulsed loads are common in portable battery-powered devices, such as mobile phones, two-way pagers and GPRS systems. The load pulses may be many times the resting current, causing a large drop in battery voltage, which can cause system shutdown.
- In cold weather, batteries are much less capable of supplying the loads than they are when warm, because of their reduced capacity and increased internal resistance.
- The large voltage drop when load pulses occur may be detrimental to the battery. Conventional capacitors usually cannot support high currents, given the space restrictions in portable electronics.
- Lithium-ion batteries may be damaged by being discharged to low voltages or by load pulses that repeatedly drop the voltage. Automatic cutout circuits may be activated.
- Effective battery run-time is reduced by the need to maintain the voltage above a threshold value at all times. When load pulses drop the voltage below the minimum level, the device must turn off.
- At the time the device shuts down, there may be much useful energy remaining in the battery.

The CAP-XX Solution

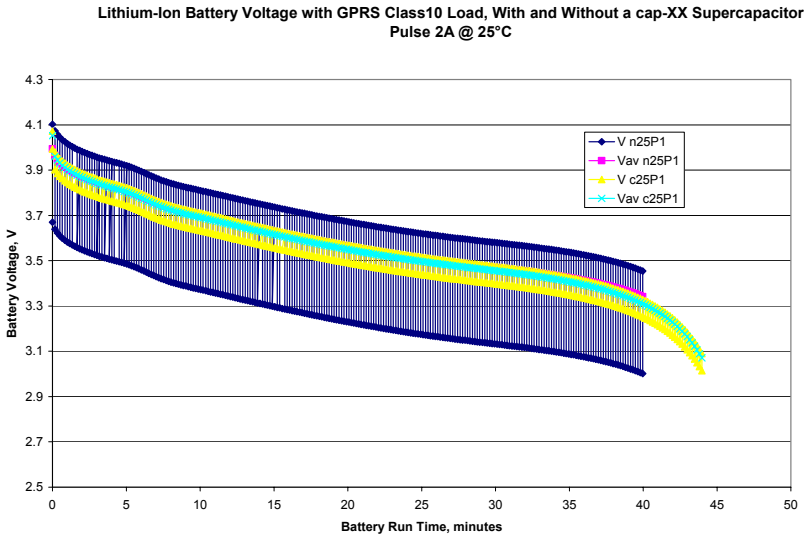
- Connect a CAP-XX supercapacitor with low ESR (equivalent series resistance) in parallel with the battery to obtain a high-performance, low-impedance hybrid with superior characteristics. CAP-XX supercapacitors can have ESRs of just a few milliohms, with capacitance from a few millifarads to Farads, and leakage currents of only a few micro-amps.
- The hybrid battery-supercapacitor can be designed to deliver the current demand during transmission pulses or other severe loads without the terminal voltage dropping to unacceptable levels. Low ESR provides CAP-XX supercapacitors with an unprecedented ability to deliver high currents.
- During the low-load intervals, the supercapacitor is re-charged by the battery.
- In low temperatures, the supercapacitor delivers the current peaks that the battery cannot.
- CAP-XX supercapacitors can be designed to suit the application, in shapes, sizes and packaging to fit the space available, such as thin prismatic forms.

The Benefits

- Reduced voltage drop during load peaks at all temperatures, resulting in extended run-time.
- Reduced source impedance compared with that of the battery alone.
- Designers can use smaller batteries than normal, with higher internal resistance, at reduced cost.
- Pulsed-load systems work in cold conditions; demanding low-temperature industrial requirements can be met.
- Effective battery capacity at low temperatures is increased.
- Low-battery thresholds can be reduced, since voltage ripple is reduced, giving increased voltage margin before shutdown occurs. This allows the battery to deliver more of its energy before shutdown, extending battery run-time.
- The possibility of damage to Lithium-ion batteries from low voltage or from high-current pulses is reduced.
- CAP-XX supercapacitors can be designed to fit the space available.

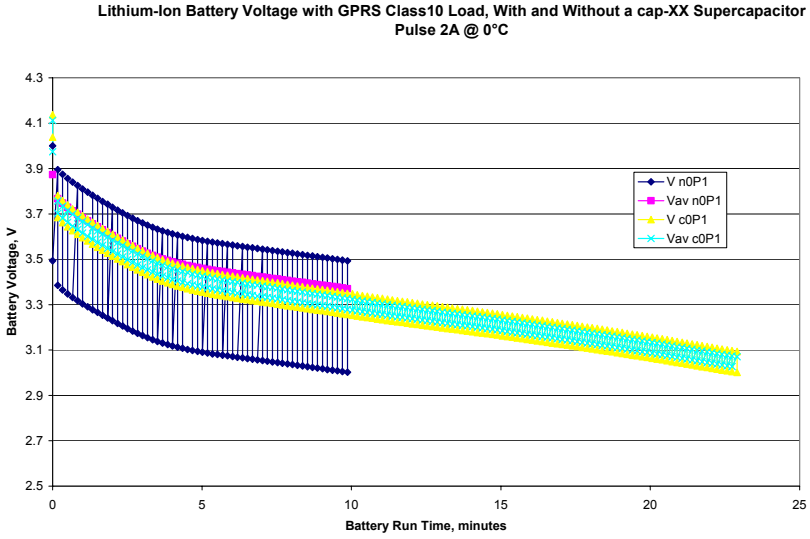
The first graph below shows the battery voltage obtained in actual tests with a 600mAh lithium-ion battery subjected to a continuous load of 100mA and a load pulse representing a 2A GPRS Class 10 (25% duty cycle, 1.154ms pulse-width) load. The battery had an internal resistance of 250mΩ, including its protection circuit. The supercapacitor used was a 0.3F, 40mΩ CAP-XX device, type GW208. The dark plot is the battery voltage without a supercapacitor in parallel. The maximum and minimum voltages on the battery are clearly seen as the dark upper and lower lines. The lighter plot in the middle is the battery voltage with the supercapacitor in parallel. (The average values of the two plots are also shown, but may not be clearly visible in print.)

The dark plot is the battery voltage without a supercapacitor in parallel. The maximum and minimum voltages on the battery are clearly seen as the dark upper and lower lines. The lighter plot in the middle is the battery voltage with the supercapacitor in parallel. (The average values of the two plots are also shown, but may not be clearly visible in print.)



The supercapacitor had a dramatic effect in reducing the voltage ripple. If the device required a minimum of 3.3V to function correctly, which is the case with some GPRS modules, then it would have shut down after 14.9 minutes without a supercapacitor. With the supercapacitor in parallel, the voltage did not drop below this threshold until 38.1 minutes into the test, 2.56 times the original run-time. This represents an effective extension in run-time of 156%. If repeating this test, the result will vary with battery type and quality.

The second graph shows the battery voltage during a test performed at 0°C, using the same test load, battery and supercapacitor as in the test above. The low temperature reduced the battery's terminal voltage, resulting in reduced headroom for the load. Again, the dark plot was the battery voltage without the supercapacitor in parallel with the battery. In cold conditions, the battery was much less able to deliver load current than it was at room temperature. Its internal resistance was increased, which increased the voltage drop at the leading edge of each pulse; its ability to maintain a steady voltage during load pulses was decreased, which resulted in increased voltage droop during load pulses. The lighter plot in the middle was the battery voltage with the supercapacitor in parallel. The total voltage ripple was reduced to a level comparable to that at room temperature. If we select the same 3.3V minimum voltage threshold for operation of the load, then it would have functioned for 1.2 minutes without the supercapacitor and 7.7 minutes with the supercapacitor, 6.42 times as long, or an increase of 542%. This result will also vary greatly with battery type and quality. However, it shows that a CAP-XX supercapacitor can make a substantial difference to a product's run-time in pulsed-load conditions and its ability to function at low temperatures.



Further Information:

CAP-XX will be pleased to supply you with detailed data and design information. Please use the contact information listed at the foot of this page.

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http://www.CAP-XX.com E-mail: sales@CAP-XX.com

Appendix C

Application Brief No. 1009 Powering GPRS Class 10 devices on PCMCIA Cards with CAP-XX supercapacitors

Application Brief No. 1010 Powering GPRS/GSM devices on CompactFlash Cards with CAP-XX supercapacitors

Application Brief No. 1011 Powering GPRS Class 12 devices on PCMCIA Cards with CAP-XX supercapacitors

CAP-XX APPLICATION BRIEF 1009

Powering GPRS Class 10 Devices on PCMCIA Cards with CAP-XX Supercapacitors

Version 1.1 24 September 2002

Outline

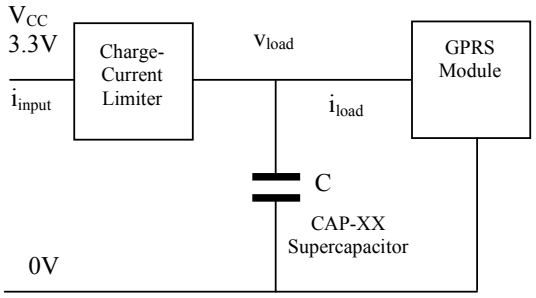
GPRS modems are now being designed into PCMCIA cards for use in notebook PCs and other products. However, the PC Card specification limits the current drain of the card to much less than a typical GPRS transmitter requires. This application brief describes a solution to this problem, using a CAP-XX supercapacitor to power the transmitter without exceeding the peak input current requirement. This improves the efficiency, while reducing costs when compared with typical solutions utilising tantalum capacitors with a DC-DC converter.

The Problem

The PC Card specification limits the peak current drawn by the card to 1Amp, while most GPRS transmitters need 1.5A to 2A to transmit at full power at 3.3V. For example, when transmitting in class 10 using a maximum of two of the eight 577µs time slots, the pulse duration is 1.154ms and the period 4.616ms. Clearly, it is not possible for the card to operate within the specification without special design measures.

The CAP-XX Solution

The diagram below shows a typical design using a CAP-XX supercapacitor that solves the problem of delivering the power needed by a GPRS transmitter, while keeping the current drawn from the PC Card interface within specification.



The CAP-XX supercapacitor has high capacitance and low ESR (equivalent series resistance), so delivers large current pulses without much change in load voltage. Because the ripple voltage on the load is small, this load-leveling effect means current drawn from the supply (the host device) during the load pulses can be under the maximum peak allowed by the PC Card specification. The most important criterion in selecting the supercapacitor is low ESR, because ESR typically contributes the most to the voltage ripple in high-C supercapacitors.

When the card is first plugged into the host, the supercapacitor is typically in a discharged state. To prevent the supercapacitor's charging current from overloading the host, a simple current-limit circuit is used, as shown above. For further information, please refer to Application Note 1002, *Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices*, from CAP-XX, available as a free download from the CAP-XX web site.

The Benefits

The low-ESR CAP-XX supercapacitor enables a transmitter to operate even though its current drain would usually exceed the value allowed by the PC Card specification. This is done with virtually 100% efficiency, instead of the lower efficiency of a DC-DC converter, and the supercapacitor does not generate EMI. The amount of energy that the host can deliver in a typical pulse period can be compared with the energy required by the load by performing a simple energy balance, as illustrated below.

If the load has a duty cycle of D (where $0<D\leq1$) and the load current has a continuous component of i_{steady} and a pulse of i_{peak} (in addition to the steady current), then the average power drawn during one cycle is:

$$P_{ave} = V_{CC}(i_{steady} + D \cdot i_{peak})$$

The maximum average power that may be drawn from the supply is given by

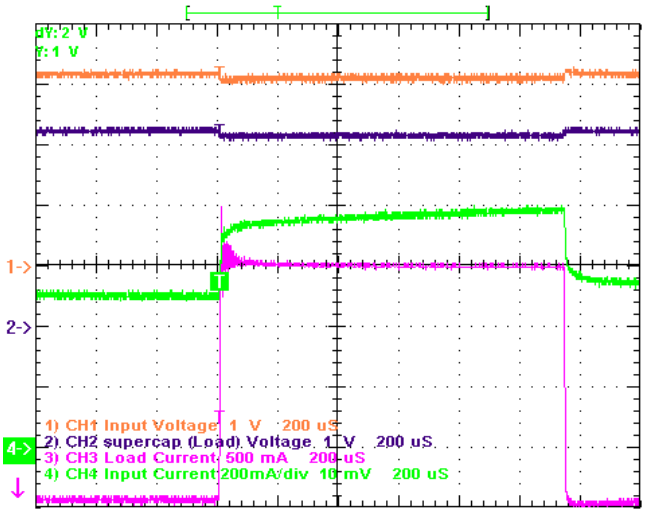
$$P_{ave,max} = V_{CC} \cdot i_{max}$$

where i_{max} is given by the PC Card specification as 1A. P_{ave} must be less than $P_{ave,max}$ for the load to function. Combining the above equations, we need the following:

$$i_{steady} + D \cdot i_{peak} < i_{max}$$

This equation is true for an ideal, infinite capacitor, so some margin must be allowed for voltage ripple in a real device. ***Example:*** Is it possible to run a transmitter in class 10 mode on a PC Card, using 2 slots out of 8 (25% duty cycle), if it draws 100mA continuously plus 1.9A peak pulse transmission current? ***Answer:*** $i_{steady} + D \cdot i_{peak} = 0.1 + 0.25 \cdot 1.9$ A = 0.575A, which is well under both the peak 1A limit and the average current limit of 0.75A. This ignores losses, but gives an approximate magnitude of the current that will be drawn from the source when using a CAP-XX supercapacitor.

Running a simple simulation can also be helpful in verifying that a load will function successfully. Spreadsheets published by CAP-XX on its web site enable one to simulate pulsed loads powered by sources with supercapacitors connected in parallel.



The oscilloscope image shows the traces from a test with a real CAP-XX supercapacitor. This was a 0.25F, 40mΩ device, type GS204. The source voltage (V_{CC}) was modeled with a 3.3V supply and 200mΩ source impedance. A 33Ω resistor was used to create the 100mA continuous load, and an electronic load imposed a 1.9A pulse for 1.154ms every 4.616ms, to simulate a class 10 (2-slot) transmission. The traces (top to bottom) are input voltage, load voltage, current drawn from host and current drawn by the GPRS module. (Zero for CH3 is the bottom graticule). Note that the host current does not exceed the 1A peak current specification and the average current is ≈ 600mA (<< 750mA allowed in the PC Card spec). It is of interest to note that increasing the source resistance or adding resistance to the current-limiter can result in a reduced peak input current, with the tradeoff of reduced minimum and average output voltage.

The table below contains a list of some CAP-XX supercapacitors that would work in the above example with a 2A maximum load current. Devices with ESRs up to 80mΩ should meet the requirements, although those with lower ESR will perform better and have more headroom. Two devices in series are required when using those with 2.3V ratings. (Contact CAP-XX for information on voltage balancing.) Besides the standard devices, CAP-XX is able to manufacture products to custom designs as well, when required.

C, Farads	ESR, mΩ	Voltage, V	Footprint, mm	Thickness, mm	Type No.
0.18	60	4.5	28.5 x 17	2.79	GW202
0.35 (each)	30 (each)	2.3	28.5 x 17	1.36	GW102 (2 req'd)
0.2	50	4.5	39 x 17	2.06	GS203
0.4 (each)	26 (each)	2.3	39 x 17	0.99	GS103 (2 req'd)

Further Information:

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CAP-XX APPLICATION BRIEF 1010

Powering GPRS/GSM Devices on CompactFlash Cards with CAP-XX Supercapacitors

Version 1.0 19 August 2002

Outline

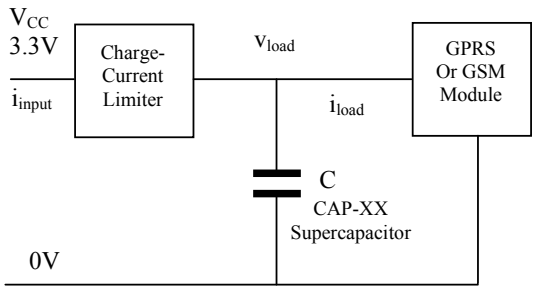
GPRS and GSM modems are now being designed into CompactFlash (CF) cards for use in PDAs and other portable devices. However, the CF card specification limits the CF+ current drain of the card to much less than a typical transmitter requires. This application brief describes a solution to this problem, using a CAP-XX supercapacitor to power the transmitter without exceeding the maximum input current requirement. This improves the efficiency, while reducing costs when compared with a solution utilising tantalum capacitors with a DC-DC converter.

The Problem

The CF Card specification limits the current drawn by a CF+ card to 0.5Amp, while most GPRS (or GSM) transmitters need 1.5A to 2A to transmit at full power at 3.3V. When transmitting in class 8 using one of eight 577µs time slots, the pulse duration is 0.577ms and the period 4.616ms. Clearly, it is not possible for the card to operate within the specification without special design measures.

The CAP-XX Solution

The diagram below shows a typical design using a CAP-XX supercapacitor that solves the problem of delivering the power needed by a GPRS/GSM transmitter, while keeping the current drawn from the CF Card interface within specification.



The CAP-XX supercapacitor has high C and low ESR (equivalent series resistance), so it delivers large current pulses without much change in load voltage. Because the ripple voltage on the load is small, this load-leveling effect means current drawn from the supply (the host device) during the load pulses can be under the maximum allowed by the CF+ Card specification. The most important criterion in selecting the supercapacitor is low ESR, because ESR typically contributes most to voltage ripple in high-C supercapacitors.

When the card is first plugged into the host, the supercapacitor is typically in a discharged state. To prevent the supercapacitor's charging current from overloading the host, a simple current-limit circuit is used, as shown above. For further information, please refer to Application Note 1002, *Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices*, from CAP-XX, available as a free download from the CAP-XX web site.

The Benefits

The low-ESR CAP-XX supercapacitor enables a transmitter to operate even though its current drain would usually exceed the value allowed by the CF Card specification. This is done with virtually 100% efficiency, instead of the lower efficiency of a DC-DC converter, and the supercapacitor does not generate EMI. The amount of energy that the host can deliver in a typical pulse period can be compared with the energy required by the load by performing a simple energy balance, as illustrated below.

If the load has a duty cycle of D (where $0<D\leq1$) and the load current has a continuous component of i_{steady} and a pulse of i_{peak} (in addition to the steady current), then the average power drawn during one cycle is:

$$P_{ave} = V_{CC}(i_{steady} + D \cdot i_{peak})$$

The maximum average power that may be drawn from the supply is given by

$$P_{ave,max} = V_{CC} \cdot i_{max}$$

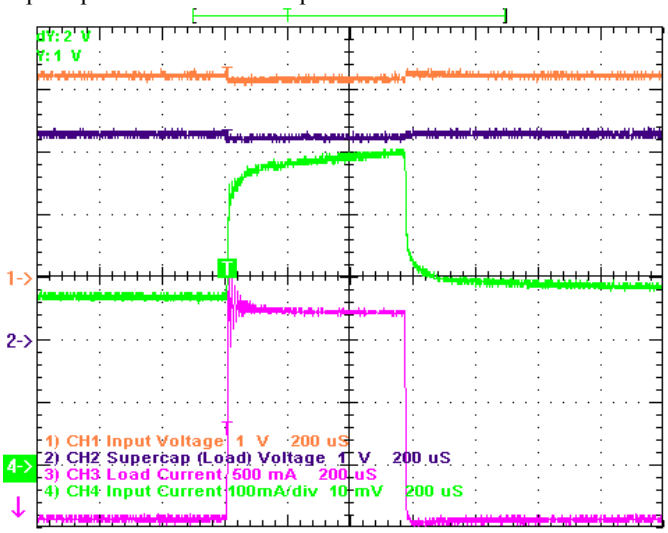
where i_{max} is given by the CF+ Card specification as 0.5A. P_{ave} must be less than $P_{ave,max}$ for the load to function. Combining the above equations, we need the following:

$$i_{steady} + D \cdot i_{peak} < i_{max}$$

This equation is true for an ideal, infinite capacitor, so some margin must be allowed for voltage ripple in a real device. ***Example:*** Is it possible to run a transmitter in class 8 mode on a CF+ Card, using 1 slot out of 8 (12.5%

duty cycle), if it draws 100mA continuously plus 1.9A peak pulse transmission current? ***Answer:*** $i_{steady} + D \cdot i_{peak}$ = 0.1 + 0.125·1.9 A ≈ 0.34 A, which is well under the 0.5A limit. This ignores losses, but gives an approximate magnitude of the current that will be drawn from the source when using a CAP-XX supercapacitor.

Running a simple simulation can also be helpful in verifying that a load will function successfully. Spreadsheets published by CAP-XX on its web site enable one to simulate pulsed loads powered by sources with supercapacitors connected in parallel.



The oscilloscope image shows the traces from a test with a real CAP-XX supercapacitor. This was a 0.25F, 40mΩ device, type GS204. (Smaller devices are also available.) The source voltage (V_{CC}) was modeled with a 3.3V supply and 200mΩ source impedance. A 33Ω resistor was used to create the 100mA continuous load, and an electronic load imposed a 1.65A pulse for 0.577ms every 4.616ms, to simulate a class 8 (1-slot) transmission. The traces (top to bottom) are source voltage, load voltage, current drawn from host and current drawn by the GPRS/GSM module. (Zero for CH3 is the bottom graticule). Note that the host current does not exceed the 0.5A specification. It is higher than the value predicted above (when ignoring resistances), but this is to be expected when taking source resistance and supercapacitor ESR into account. In a real application, one of the CAP-XX supercapacitors with a lower ESR (or a custom-designed type) would be used, to allow for some headroom and/or to support a transmitter that drew a higher current. When simulating this example with the CAP-XX spreadsheet, the source current exceeds the specified value. This is because the lab test benefited from stray inductance and resistance in the supply leads and in the current-limiter, which result in more current being drawn from the supercapacitor than approximate calculations or modeling would suggest. Both testing and simulation should be performed, to confirm that the design meets the specifications.

The table below contains examples of CAP-XX supercapacitors that would work in the above example without exceeding the 0.5A limit, with the maximum load currents shown. Two devices in series are required when using those with 2.3V ratings. (Contact CAP-XX for information on voltage balancing.) Besides the standard devices, CAP-XX is able to manufacture products to custom designs as well, when required.

Max i_{load}, A	C, Farads	ESR, mΩ	Voltage, V	Footprint, mm	Thickness, mm	Type No.
1.75	0.45	24	4.5	39 x 17	3.9	GS205
1.75	0.95	12	2.3	39 x 17	1.91	GS105 (2 req'd)
1.65	0.35	32	4.5	28.5 x 17	4.63	GW210
1.65	0.65	16	2.3	28.5 x 17	2.28	GW110 (2 req'd)

Further Information:

CAP-XX will be pleased to supply detailed data and design information. For further details, please use the contact information listed at the foot of this page.

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CAP-XX APPLICATION BRIEF 1011

Powering GPRS Class 12 Devices on PCMCIA Cards with CAP-XX Supercapacitors

Version 1.1 24 September 2002

Outline

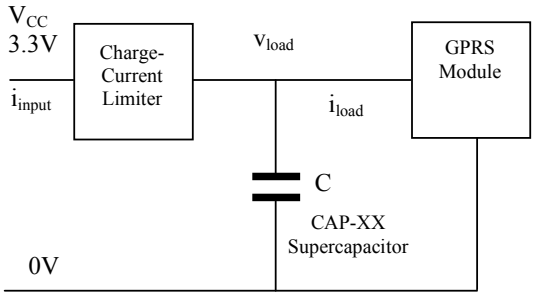
GPRS modems are now being designed into PCMCIA cards for use in notebook PCs and other products. However, the PC Card specification limits the current drain of the card to much less than a typical GPRS transmitter requires. This application brief describes a solution to this problem, using a CAP-XX supercapacitor to power the transmitter without exceeding the peak input current requirement. This improves the efficiency, while reducing costs when compared with typical solutions utilising tantalum capacitors with a DC-DC converter.

The Problem

The PC Card specification limits the peak current drawn by the card to 1Amp, while most GPRS transmitters need 1.5A to 2A to transmit at full power at 3.3V. For example, when transmitting in class 12 using a maximum of four of the eight 577µs time slots, the pulse duration is 2.308ms and the period 4.616ms. Clearly, it is not possible for the card to operate within the specification without special design measures. The relatively high duty cycle imposes a limit on the current the transmitter can draw.

The CAP-XX Solution

The diagram below shows a typical design using a CAP-XX supercapacitor that solves the problem of delivering the power needed by a GPRS transmitter, while keeping the peak current drawn from the PC Card interface within specification.



The CAP-XX supercapacitor has high capacitance and low ESR (equivalent series resistance), so delivers large current pulses without much change in load voltage. Because the ripple voltage on the load is small, this load-leveling effect means current drawn from the supply (the host device) during the load pulses can be under the maximum allowed by the PC Card specification. The most important criterion in selecting the supercapacitor is low ESR, because ESR typically contributes the most to the voltage ripple in high-C supercapacitors.

When the card is first plugged into the host, the supercapacitor is typically in a discharged state. To prevent the supercapacitor's charging current from overloading the host, a simple current-limit circuit is used, as shown above. For further information, please refer to Application Note 1002, *Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices*, from CAP-XX, available as a free download from the CAP-XX web site.

The Benefits

The low-ESR CAP-XX supercapacitor enables a transmitter to operate even though its current drain would usually exceed the value allowed by the PC Card specification. This is done with virtually 100% efficiency, instead of the lower efficiency of a DC-DC converter, and the supercapacitor does not generate EMI. The amount of energy that the host can deliver in a typical pulse period can be compared with the energy required by the load by performing a simple energy balance, as illustrated below.

If the load has a duty cycle of D (where $0<D\leq1$) and the load current has a continuous component of i_{steady} and a pulse of i_{peak} (in addition to the steady current), then the average power drawn during one cycle is:

$$P_{ave} = V_{CC}(i_{steady} + D \cdot i_{peak})$$

The maximum average power that may be drawn from the supply is given by

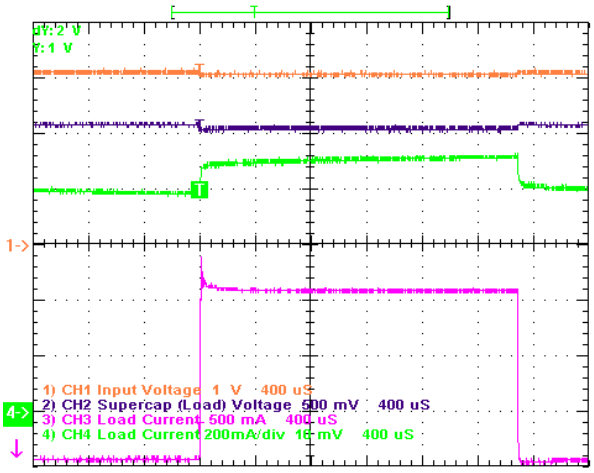
$$P_{ave,max} = V_{CC} \cdot i_{max}$$

where i_{max} is given by the PC Card specification as 1A. P_{ave} must be less than $P_{ave,max}$ for the load to function. Combining the above equations, we need the following:

$$i_{steady} + D \cdot i_{peak} < i_{max}$$

This equation is true for an ideal, infinite capacitor, so some margin must be allowed for voltage ripple in a real device. ***Example:*** Is it possible to run a transmitter in class 12 mode on a PC Card, using four slots out of eight (50% duty cycle), if it draws 100mA continuously plus 1.8A peak pulse transmission current? ***Answer:*** $i_{steady} + D \cdot i_{peak} = 0.1 + 0.5 \cdot 1.8$ A = 1.0A, which is at the 1A peak current limit. This ignores losses, so a 1.8A pulse is the maximum that could be supported in an ideal circuit. In a real circuit, the pulse load that can be supported will necessarily be less, such as 1.5A. (A 1.5A pulse results in an average of 0.85A, which leaves some headroom and allowance for losses.)

Running a simple simulation can also be helpful in verifying that a load will function successfully. Spreadsheets published by CAP-XX on its web site enable one to simulate pulsed loads powered by sources with supercapacitors connected in parallel.



The oscilloscope image shows the traces from a test with a CAP-XX supercapacitor, rated 0.48F, 20mΩ. The source voltage (V_{CC}) was modeled with a 3.3V supply and 200mΩ source impedance. A 33Ω resistor was used to create the 100mA continuous load, and an electronic load imposed a 1.5A pulse for 2.308ms every 4.616ms, to simulate a class 12 (4-slot) transmission. The traces (top to bottom) are input voltage, load voltage, current drawn from host and current drawn by the GPRS module. (Zero for CH2 and CH3 is the bottom graticule). Note that the host current does not exceed the 1A peak current specification and the load voltage remains above 3V. Adding extra source resistance can reduce the maximum current drawn from the source, but it is not advisable in applications in which the load voltage is close to the minimum.

The table below contains a list of some CAP-XX supercapacitors that would work in the above example with a 1.6A maximum load current. Care should be taken to keep trace resistances to the minimum, particularly on the load side of the supercapacitor, if it is important to keep the operating voltage of the load above 3V. The lower the resistances and the ESR of the supercapacitor used, the better the ripple voltage will be and the more voltage headroom there will be. Two devices in series are required when using those with 2.3V ratings. (Contact CAP-XX for information on voltage balancing.) Besides the standard devices, CAP-XX is able to manufacture products to custom designs as well, when required.

C, Farads	ESR, mΩ	Voltage, V	Footprint, mm	Thickness, mm	Type No.
0.45	24	4.5	39 x 17	3.9	GS205
0.95 (each)	12 (each)	2.3	39 x 17	1.91	GS105 (2 req'd)
1.4	20	4.5	39 x 17	4.99	GS208
2.7 (each)	10 (each)	2.3	39 x 17	2.46	GS108 (2 req'd)

Further Information:

CAP-XX will be pleased to supply detailed data and design information. For further details, please use the contact information listed at the foot of this page.

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Appendix D

CAP-XX Application Note 1003

The Supercapacitor Solution to GPRS and Other Pulsed Loads on CompactFlash and PC Cards

CAP-XX APPLICATION NOTE No. 1003

The Supercapacitor Solution to GPRS and Other Pulsed Loads on CompactFlash and PC Cards

Revision 1.0, December 2002

Outline

CompactFlash and PC Card products are now being designed with pulsed-load subsystems, such as GPRS and GSM modules. These subsystems frequently require peak currents that exceed the level allowed by the CF Card specification for CF+ devices or the PC Card specification. A CAP-XX supercapacitor is a solution to providing the peak power while keeping the current drawn from the host within specification. This application note describes simple host equivalent circuits, power-up and charging of the supercapacitor, voltage ripple and peak current demand, some of the relevant equations, and a spreadsheet tool available from CAP-XX to assist with modelling and development work.

The Problem

The CompactFlash specification allows a CF+ card to draw only 0.5A (maximum average RMS current) and this may be drawn only after switching to Power Level 1. On power-up, the card must operate in Power Level 0, in which it must not exceed 75mA at 3.3V, or 100mA at 5V, if it is to meet the specification.

The PC Card specification (Release 8) allows a PC Card to draw the following currents from V_{CC}, when operating at 5V (minimum 4.75V): 0.66A peak (averaged over any 10ms period) and 0.5A average (averaged over any 1s period). If the host supports it, then when operating at 3.3V (minimum 3.0V), the card may draw 1A peak (averaged over any 10ms period) and 0.75A average (averaged over any 1s period).

Typical GPRS and GSM transmitters require much higher currents than the peak values allowed by the specifications above. Therefore, if the load is to function correctly, then the card must be able to store much of the energy required by the load and recharge itself between load pulses, so that it presents a smoothed load to the host. See References 2 and 3.

A low-ESR (equivalent series resistance) CAP-XX supercapacitor can store the energy needed by the load and deliver it on demand. However, it needs to be charged on power-up once the PC or CF card has been set at the correct power level. This can overload the host if charging is not controlled. In certain applications, if the load draws a particularly high current, there may also be a requirement to dynamically limit the current drawn from the host during operation.

The card therefore needs a means of controlling the start-up operations, the charging of the supercapacitor, and any current-limiting required during operation.

The CAP-XX Solution

Circuit Configuration

A CAP-XX supercapacitor across the power supply provides the solution to delivery of a high-power pulse. Relatively simple circuits can provide the solution to charging the supercapacitor at the right time and at the right rate, so that the host device is not overloaded. These are described in more detail below. The card may also incorporate a DC-DC converter, which may be necessary if the load needs to operate at a different voltage from that provided by the host, or if the load voltage has stability requirements that can only be met with a regulated output.

The power supply from the host device is assumed to conform to the CF Card or PC Card specification. It can be regarded as having one of the equivalent circuits in Figure 1.

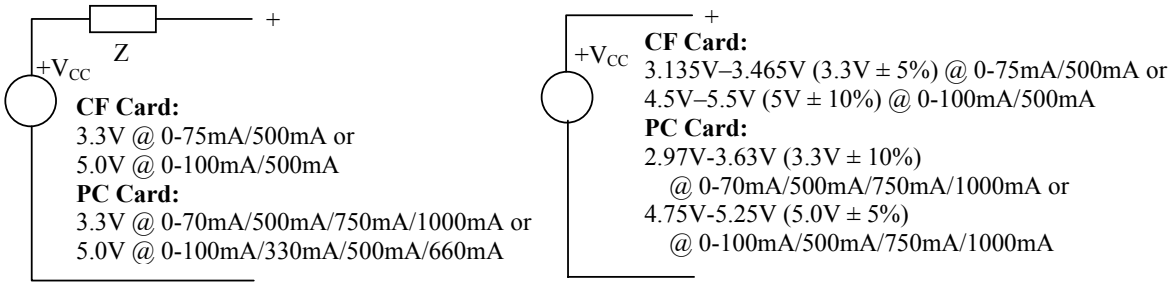

Figure 1 Power Source Equivalent Circuits

The circuit on the left in Figure 1 is known as the Thevenin equivalent circuit representing a linear circuit that has a particular open-circuit voltage and a known short-circuit current (or a known, reduced output voltage at a known current). It is often more useful than the circuit on the right, although both have advantages. The voltages and currents shown were taken from the relevant CF Card (CF+) and PC Card specifications. The current values for a CF Card refer to the low-power 'Power Level 0' state and the higher 'Power Level 1' state that applies only to CF+ devices. The current values for a PC Card refer to the card-configuration current (the lowest value), the static current, the average current and the peak current (as given in Release 8 of the specification).

Note that some older PC Card host devices that may still be in use could supply 5V to the card and not 3.3V, even if the card is configured for 3.3V.

The impedance, Z, in Figure 1 is typically assumed to be a resistor. Its value (R) is usually calculated from the values of the open-circuit and loaded output voltages, for a known load current, as follows:

$$R = (V_{CC,Open} - V_{CC,Loaded})/I_{Load} \qquad (1)$$

To use equation 1, a load is imposed that is not excessive for the source, and the voltage under load ($V_{CC,Loaded}$) is measured.

The circuit on the right in Figure 1 represents a simple voltage source that has a range of outputs that depends on the load, the time at which the load current is applied (on power-up or later) and on whether the host system supplies 5V or 3.3V.

The approximate **maximum** values of the Thevenin source impedance, Z, can be calculated from the values given in the specification. For a CF card at 3.3V, it is

$$R = (3.465 - 3.135)/0.5 = \mathbf{0.66\Omega} \text{ (Power Level 1)}$$

For a CF card at 5V, the approximate maximum source impedance is

$$R = (5.5 - 4.5)/0.5 = \mathbf{2\Omega} \text{ (Power Level 1)}$$

In practice, the source impedance of the PC Card or CF Card power supply is considerably less than the maximum values. Source impedances in the range of 100mΩ - 200mΩ are typical.

Figure 2 shows a basic power system in which a supercapacitor is connected in parallel with the supply. The supercapacitor is represented by a simple model consisting of its capacitance, C, in series with its ESR, R_C. (Note that this is not an added resistor; the resistance in the supercapacitor connection should be kept as low as possible in all circuits.) The supply is modelled as a voltage source, V_{CC} (or V_B), in series with its source resistance, R.

When the device is first connected to the supply (the host) with a discharged supercapacitor, the supercapacitor's low ESR and high C can result in a large current being drawn from the supply. The current-limiter block represents a circuit that charges the supercapacitor without violating the power-drain specifications of the host device. This circuit may also limit the current during normal use, if high load pulses would otherwise make the card exceed the maximum current allowed. The current-limiter circuit will include components, such as a MOSFET, that add to the series resistance of the circuit; for modelling purposes, this resistance may be added to that of the supply's source impedance. The current-limiter may have a control input that tells it when to start charging the supercapacitor and possibly also when to turn off supply to the supercapacitor. This control signal would be under the control of the software running on the card. E.g., in a CF card it could activate the current-limiter when the host device permitted the card to go to Power Level 1.

For further information on current-limiting circuits, see References 1 and 4.

The circuit in Figure 2 would typically be chosen as a low-cost implementation. Refer to reference 1 for examples of such a circuit. Figure 7 shows a simulation of waveforms in a PC Card circuit of this type transmitting a class 10 GPRS signal. Note that the low ESR and high C of the supercapacitor result in a small ripple voltage, which is well under the 300mV – 400mV maximum allowed by the specifications of many GPRS modules.

If the current drawn by the load during pulses is so high that current-limiting is necessary during operation even with the supercapacitor present, then a current-limit circuit that is always operational is needed, as opposed to a current-limit circuit that only limits the current during power-up. Note that the current limit reduces the average voltage at the supercapacitor to less than the output voltage of the supply. However, provided there is sufficient average current and no limiting between load pulses, the low ESR and high C of the supercapacitor maintain the minimum voltage to the RF power amplifier module, and the voltage ripple is less than the maximum allowed at the power input to the module.

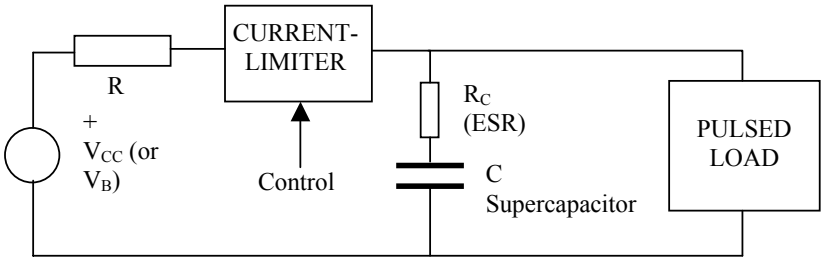

Figure 2 Basic Power System With Supercapacitor

Figure 3 is a power system in which a DC-DC converter is used to increase the flexibility of the system. It could be a buck or boost converter, depending on the requirements of the load. This circuit would be selected when the load must be able to operate at a voltage that is substantially different to the source voltage, for example, with GPRS modules whose maximum V_{CC} or V_{Batt} is 4.5V but minimum V_{CC} or V_{Batt} during transmission is 3.3V. This means their operating voltage range is too low for the 5V rail (maximum 5.5V on a PC card, or 5.25V on a CF card) and too high for the 3.3V rail (minimum 2.97V on a PC card, or 3.135V on a CF Card).

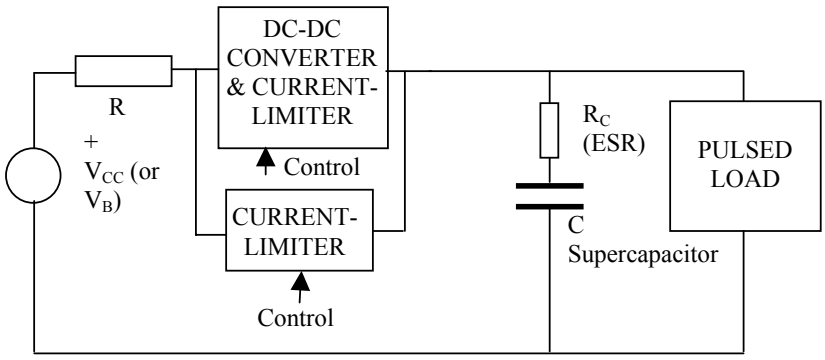

Figure 3 Power System With DC-DC Converter and Supercapacitor

For example, if the load requires a low voltage, such as 3.3V, a buck converter with current-limited output may be used to reduce a 5V input to 3.3V. When the input is 3.3V, the converter would be bypassed and the current-limiter circuit would be used to charge the supercapacitor and supply the load. The current-limiter would only be required to limit the current during normal operation if not doing so resulted in the current drawn from the host exceeding the allowed value. As this would depend on the source impedance of the host, it may be necessary to test the card in the relevant conditions and/or simulate the circuit.

If the load in Figure 3 requires a higher voltage, such as 4.5V, a boost converter with current-limited output may be used to boost 3.3V to the required level. To operate from a 5V input, the boost converter would be bypassed and the load would be supplied by the current-limiter, which would incorporate a LDO (low drop-out) regulator to prevent the output exceeding either the supercapacitor's or the load's rated voltage.

The control signals would activate either the current-limiter or the DC-DC converter, depending on the value of the input voltage. This would be under software control and would occur when the host permitted the card to change to Power Level 1.

The configuration in Figure 3 has the advantage that the supercapacitor can supply most (or all) of the load pulse, so the DC-DC converter need only be capable of supplying the average load current plus losses. The power MOSFETs and the inductor in the DC-DC converter can therefore be much smaller than they would need to be to supply the peak current.

In Figure 3, the output of the DC-DC converter must be current-limited, so that the supercapacitor supplies most of the peak current and the DC-DC converter does not overload the host during load pulses. Without current-limiting, the DC-DC converter will try to maintain the voltage at its output (assuming the source can supply sufficient current), and not enough current will be drawn from the supercapacitor. (For any capacitor, the current flow in or out is $i = C(dv/dt)$; i.e., there has to be a change in voltage for it to supply any current. With a high-C supercapacitor, this voltage change does not have to be large for it to provide a substantial current.)

Figure 4 shows a configuration that may be advantageous when the load requires a very stable

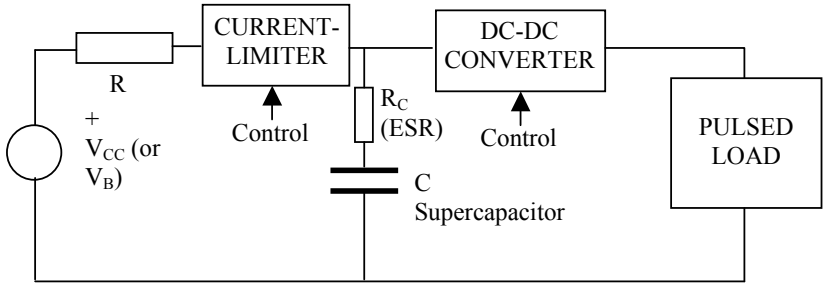

Figure 4 Power System With Stable DC-DC Converter Output and Supercapacitor

supply voltage, and/or when the load voltage must be different to the input voltage, and/or when the peak current must be maintained for so long that the supercapacitor voltage would drop below the minimum voltage the load requires. The current-limiter charges the supercapacitor, which supplies the DC-DC converter. The stability of the load voltage is therefore determined by the DC-DC converter. The supercapacitor voltage may be allowed to drop significantly during load pulses, provided it does not drop below the minimum required by the DC-DC converter. The current-limiter ensures that the host is not overloaded during initial charging of the supercapacitor and, if necessary, during operation. If the benefits justify it, the current-limiter may be a DC-DC converter that is capable of operating as a current-limiter. This option depends on whether sufficient space is available if this provides sufficient additional efficiency to justify it. (If limiting during normal operation is necessary, then the designer will need to compare the efficiency of a DC-DC converter acting as a limiter, which may be 80%-90+%, with that of a linear limiter that has a voltage drop across it at least for some of the time.)

A disadvantage of the Figure 4 configuration is that the DC-DC converter has to be able to provide the full peak current required by the load, which increases the sizes of the MOSFETs and inductor over those required for the configuration of Figure 3.

Refer to the CAP-XX Application Note 1002, Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices, for more information on current-limiting circuits.

Circuit Design and Modelling

Introduction

A useful tool for modelling pulsed-load circuits is a spreadsheet developed by CAP-XX that can be downloaded free-of-charge from its web site. (See URL at the end of this document.) The version on the web site is in two parts, one of which is designed to simulate loads that draw a fixed current during the pulse, and the other for loads that draw a fixed power during the pulse. The latter type of load dynamically increases the current drawn from the supply as the voltage drops, which can be an important characteristic of some loads that need to output a certain power. These simulator spreadsheets can be used as a design aid and to get an indication of whether a circuit will behave within specification. SPICE simulations of a proposed design may also be very helpful.

Figure 5 is the equivalent circuit of the power source (which could be a battery) and the supercapacitor. The load is shown as a pulse of either a given current or a given power that is imposed at a given frequency. In order to make sure the system meets a specification, it is necessary to be able to determine the peak current drawn from the source.

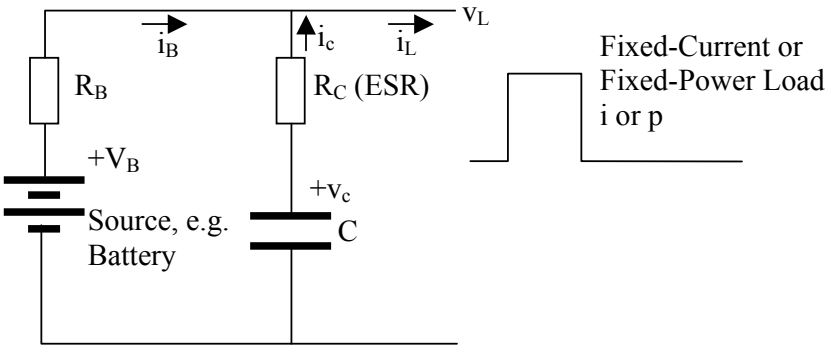

Figure 5 Simple Equivalent Circuit of Power Source and Supercapacitor Subjected to Pulsed Load

Fixed-Current Pulse

In a circuit in which there is **no supercapacitor** (C) in parallel with the battery, the open-circuit (no-load) voltage of the system is V_B. The voltage under load is given by the following:

$$v_L = V_B - i_L R_B \qquad (2)$$

If a load pulse of a certain current is drawn with no supercapacitor connected, the power delivered to the load is given by the following:

$$p_L(t) = [V_B - i_L(t) \cdot R_B] i_L(t) \qquad (3a)$$

$$= [V_B - I_{pulse} R_B] I_{pulse} \quad \text{(during load pulse)} \qquad (3b)$$

This is the difference between the power delivered by the source (battery or power supply) and the losses in its internal resistance. Placing a low-ESR supercapacitor in parallel with the battery can greatly reduce the amount of voltage drop during load pulses. This increases the power delivered to the load.

The charge (in Coulombs) drawn from the battery by each load pulse depends only on the current and the pulse duration, not on the battery voltage. The voltage on the ideal "internal" battery, excluding the internal resistance, remains unchanged during the pulse. If the internal resistance behaved in all respects like a real resistor, including dissipating power when carrying current, then the battery would be delivering the same energy in total, where the "load" is considered to include its own internal resistance. Obviously, the energy delivered to the real load would then be reduced by the amount lost in the internal resistance. The actual behaviour of the internal resistance of a battery may depend on the battery's chemistry and its design.

Consider a system with a supercapacitor in parallel with the power source (as above) that has been left to reach equilibrium for a long time. At equilibrium, with no external load, $v_C = V_B$. It can be shown that, for a current pulse that is drawn by a load, the current in the supercapacitor will obey the following equation for the duration of the pulse:

$$i_C(t) = I_{pulse} \frac{R_B}{R_B + R_C} \cdot e^{-\frac{t}{(R_B + R_C)C}} \qquad (4)$$

where I_{pulse} is the magnitude of the current pulse. This equation applies regardless of the voltage at the voltage source. Obviously, the higher the initial source (or battery) and supercapacitor voltage, the greater will be the energy drawn from the system during the pulse, since the power drawn at any instant is equal to the product of voltage and current. From the above, the initial current in the supercapacitor when the pulse is applied will be as follows:

$$i_C(0) = \frac{R_B}{R_B + R_C} I_{pulse} \qquad (5)$$

The following relationship applies to the currents:

$$i_B(t) = i_L(t) - i_C(t) \qquad (6)$$

Thus, the current drawn from the power source and the current's initial value will be defined by the following:

$$i_B(t) = I_{pulse}[\frac{R_C}{R_B + R_C} \cdot e^{-\frac{t}{(R_B + R_C)C}}] \quad (7)$$

$$i_B(0) = I_{pulse}[\frac{R_C}{R_B+R_C}] \quad (8)$$

If R_C is very much smaller than R_B, the supercapacitor will provide the majority of the initial current. If C is sufficiently large, then the supercapacitor will continue to provide the majority of the current for the duration of the pulse. Typically, CAP-XX supercapacitors are designed to be large enough in most applications to deliver a substantial part of the load current, with the result that there is very little ripple voltage on the load. If the system is in equilibrium before the pulse is applied, then the output (load) voltage obeys the following equation for the duration of the current pulse:

$$v_L(t) = V_B - I_{pulse} \cdot R_B[\frac{R_C}{R_B + R_C} \cdot e^{-\frac{t}{(R_B + R_C)C}}] \quad (9)$$

This equation shows that the smaller R_C is in relation to R_B, the smaller will be the initial voltage drop when the load pulse is applied. The larger the value of C, the longer the time constant, $(R_B+R_C)C$, and the less will be the voltage droop at the output over the duration of the current pulse.

If the current pulses are repeated at regular intervals, it can be shown that the average voltage on the "ideal" supercapacitor, C, (the internal equivalent ideal capacitance) will be equal to the average voltage at the output, as follows:

$$v_C(ave) = v_L(ave) = V_B - R_B \cdot i_L(ave) \quad (10)$$

Note that the greater the duty cycle (or mark-space ratio) of the pulse waveform, the more the average current approaches the maximum (peak) current, and the closer the average voltage gets to the voltage under load of the power source alone. At 100% duty cycle, the average voltage equals the voltage of the battery alone under load.

If C is sufficiently large and R_C sufficiently small, the fluctuations in voltage on the supercapacitor during the load pulses and the intervals between pulses will be small. The supercapacitor has the effect of a first-order filter on the voltage that is very effective by virtue of its large C and small ESR, thereby smoothing the ripple. (This is also known as load-levelling.) Since the power that can be delivered to the load depends on the output voltage, the supercapacitor enables the system to supply increased power to the load, compared with the ability of the power source alone, by maintaining the voltage level during the load pulses.

The voltage drop under load (with a duty cycle under about 0.5) can be significantly reduced by the use of a supercapacitor in parallel with the power source. This is shown by the following equations and example, in which it is assumed that *all load current* for the duration of the pulse is drawn from the supercapacitor. Adding the supercapacitor's resistive (ESR) voltage drop and capacitive voltage drop, a rough approximation to the total voltage drop during a pulse is given by the following:

$$V_{drop} = I_{pulse}(R_C + \frac{T_{ON}}{C}) \quad (11)$$

where T_{ON} is the pulse length in seconds. If the power source remains connected to the load during the application of the load pulse(s), then it will assist in maintaining the voltage, and the drop will be less than that given by this equation. In some applications, it may be desirable to disconnect the source during the pulse, as this can assist in isolating other circuits from an electrically noisy load.

Example: A supercapacitor is rated at 0.5F, 20mΩ, and the pulse is 2A for 577μs. Using the above equation for the supercapacitor alone, the total voltage drop during a single pulse on the output would be 42mV. With the power source connected, the value would be even less. By comparison, if the source had an internal resistance of 100mΩ, which is not atypical, the voltage drop on the internal resistance would be 200mV if no supercapacitor were present. Many small batteries actually have much higher internal resistance than this value.

If the load pulses were 577μs long and repeated at 217Hz (period 4.61ms, 12.5% duty cycle), e.g. GSM transmitter pulses, then the average current would be 0.25A, and the average voltage on the supercapacitor (and on the load) would be 25mV less than V_B. The maximum voltage drop with a supercapacitor present would again be less than 42mV (with the source connected), compared with 200mV for the source alone. This neglects the small voltage existing across the ESR of the supercapacitor towards the end of the "off" period, when the source is recharging the supercapacitor. This is usually not a bad approximation, since the recharging current by then is typically small relative to the load current.

The power delivered to the load without a supercapacitor is defined by equation 3. When a supercapacitor is in parallel with the power source, the load voltage is relatively constant, and the following is a good approximation to the power delivered to the load:

$$\begin{aligned} p_L &\cong v_L(ave) \cdot i_L(t) \\ &= v_L(ave) \cdot I_{pulse} \qquad \text{(during constant-current pulse)} \\ &= [V_B - R_B \cdot i_L(ave)] \cdot I_{pulse} \\ &= (V_B - R_B \cdot I_{pulse} \cdot D) \cdot I_{pulse} \qquad (0 \le D \le 1) \end{aligned} \qquad (12)$$

where D is the duty cycle of the pulsed load waveform. This approximation breaks down if there is a lot of voltage ripple, particularly if the supercapacitor's ESR is large or its capacitance is small.

The following is the approximate difference between the power delivered to the load during a pulse without a supercapacitor and with a supercapacitor, provided voltage ripple is small:

$$p_{diff} \cong R_B \cdot I^2_{pulse} - R_B \cdot I^2_{pulse} \cdot D$$

or

$$p_{diff} \cong R_B \cdot I^2_{pulse} \cdot (1 - D) \qquad (13)$$

The energy delivered to the load during each pulse differs in the two cases (with and without a supercapacitor) by the above value multiplied by the pulse width in seconds, as follows:

$$e_{diff} \cong R_B \cdot I^2_{pulse} \cdot (1 - D) \cdot T_{ON} \qquad (14)$$

where e_{diff} is the difference in energy delivered to the load during a constant-current pulse with and without a supercapacitor in parallel with the battery, and T_{ON} is the pulse duration in seconds.

Another approach to a consideration of the energy flows is to examine the difference between the power/energy output from the ideal battery/source (V_B) with and without a supercapacitor. Obviously, when a supercapacitor is used, the power output of the battery during a pulse is less than it would be without one. This must be so because the voltage dropped across R_B is reduced during the pulse, owing to the reduced current flow from the battery and the higher output voltage during the pulse. However, the battery continues to discharge into the supercapacitor when the load pulse is off, thus recharging it, but draining further energy from the battery.

If the supercapacitor is initially charged by the battery, it delivers no net charge to the load. Therefore, if we neglect the charge remaining in the supercapacitor when the battery is depleted, the total charge delivered by the battery is the same whether a supercapacitor is present or not, and the total energy delivered by the battery to R_B and the load (combined) is also the same. The situation is different when the load draws a fixed power during the pulses instead of a fixed current

If the instantaneous internal (or open-circuit) voltage on the supercapacitor is v_C, the source voltage is V_B, the current out of the battery is i_B and current out of the supercapacitor is i_C, then it can be shown that the following equations describe the dynamic behaviour of the circuit:

$$i_C = \frac{v_C - V_B + i_L R_B}{R_B + R_C} \quad (15)$$

$$i_B = i_L - i_C = \frac{V_B - v_C + i_L R_C}{R_B + R_C} \quad (16)$$

$$\Delta v_C = -\frac{i_C \cdot \Delta t}{C} \quad (17)$$

where i_C is considered positive when current flows out of the supercapacitor, as shown in Figure 5. Δt is the time step in the simulator. The value of v_C at the next time step is given by:

$$v_C(n+1) = v_C(n) + \Delta v_C \quad (18)$$

If a current limit, I_{Lim}, is specified and if $i_B > I_{Lim}$ in the simulation, then i_B is set equal to $I_{Lim,}$ and v_c is calculated as follows:

$$v_c = V_B + i_L R_C - I_{Lim}(R_B + R_C) \quad (19)$$

These equations can be used to create a simulation of the circuit's response to a given load current, i_L, or can be solved analytically to obtain equations describing the response to a given load waveform. They form the basis of the simulator built into the fixed-current pulsed-load simulator spreadsheet available from the CAP-XX web site. The following equations define the instantaneous values of the load voltage, the power delivered to the load, the power loss in the internal resistance of the battery and the power loss in the ESR of the supercapacitor:

$$v_L = V_B - i_B \cdot R_B \quad (20)$$

$$p_L = v_L \cdot i_L \quad (21)$$

$$p_{R_B} = {i_B}^2 \cdot R_B \quad (22)$$

$$p_{R_C} = {i_c}^2 \cdot R_C \quad (23)$$

The energy expended or delivered in a time Δt in any of the above three power relationships is determined from following simple equation:

$$e = p \cdot \Delta t \quad (24)$$

At the time the first pulse of a repeated pulsed load is applied, the supercapacitor's internal voltage is the same as the voltage on the battery, provided the supercapacitor has had sufficient time to charge. With each applied pulse, the voltage on the supercapacitor drops slightly, until its average voltage (in steady-state) reaches the average value given by equation 10.

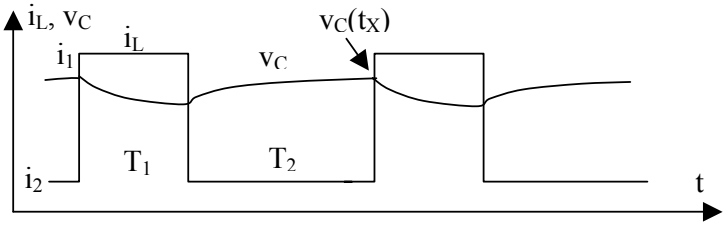

Figure 6 Determination of Open-Circuit Supercapacitor Voltage at Leading Edge of Fixed-Current Load Pulse

Figure 6 shows a train of load pulses after the supercapacitor has reached steady state. The graphs are the idealised load current (the rectangular wave) and the voltage ripple on the supercapacitor (exaggerated in scale for the sake of clarity). It can be shown that the **open-circuit** voltage on the supercapacitor at the leading edge of a load pulse in steady-state conditions is given by the following equation:

$$v_C(t_X) = \frac{R_B(i_2 - i_1)\cdot e^{\frac{-T_2}{C(R_B+R_C)}} + (i_1 R_B - V_B)\cdot e^{\frac{-(T_1+T_2)}{C(R_B+R_C)}} + V_B - i_2 R_B}{1 - e^{\frac{-(T_1+T_2)}{C(R_B+R_C)}}} \quad (25)$$

The voltage $v_C(t_X)$ will be different to the voltage observed at the supercapacitor's terminals by an amount equal to $R_C i_C$ at the instant of measurement. $v_c(t_X)$ is the value required for "Vinit Supercap" in the Fixed-Current Pulse Simulator.

Examples on the use of the Fixed-Current Pulsed-Load Simulator are included in the section titled *Determination of C and ESR Required.*

Fixed-Power Pulse

Refer again to the equivalent circuit in Figure 5. This discussion deals with a load that requires pulses of power that are essentially constant for the duration of the pulses. The load may be a GSM or GPRS transmitting device for example, or one of many other devices. A computer's CPU may also present an approximate rectangular power waveform when operating in thermal throttling mode.

If the power source is a reasonably fresh battery or a power supply and if there is no supercapacitor present, the voltage will remain relatively constant during each load pulse after the initial voltage drop. However, the initial voltage drop, equal to $i_L R_B$ (for a battery), will be very much larger than it would be with a supercapacitor present. The current drawn during the pulse remains relatively constant because the power drawn is constant and the voltage is almost constant. If the battery voltage continues to drop during the load pulses, the load will draw increasing current in order to keep the power constant.

To simplify the equations, the following approximation may be used: The power to the load is approximately $p_L = V_B\, i_L$. The approximate current drawn by the load is

$$i_L = \frac{p_L}{v_L} \approx \frac{p_L}{V_B - \frac{p_L}{V_B} R_B} \quad (26)$$

In the above equation, the power delivered to the load is reduced by the voltage drop across the internal resistance of the battery. This, in turn, means that the load has to draw an increased current in order to receive the required power, hence increasing the current demand over that of an ideal system in which the battery has zero internal resistance.

As the output voltage, v_L, drops, the current drawn by the load increases, as it must, in order to maintain the required power.

The exact relationship between the load current in a system with no supercapacitor and the power required by the load is given by the following equation:

$$i_L(t) = \frac{V_B \pm \sqrt{V_B{}^2 - 4\,p_{pulse}(t) \cdot R_B}}{2R_B} \qquad (27)$$

If there is a supercapacitor in parallel with the battery, then the voltage drop under load will be reduced, as discussed before. This has the effect of reducing the current required to deliver the power to the load. This, in turn, assists in reducing the voltage ripple that is already reduced by the presence of a supercapacitor.

With a supercapacitor in parallel with the power source, the output voltage under load may be approximated by the average voltage, and this is determined from the average power. For a load pulse of a given power, p_{pulse}, and a given duty cycle, D ($0 \le D \le 1$), the average power is the product

$$p_L(ave) = p_{pulse}D \qquad (0 \le D \le 1) \qquad (28)$$

If the supercapacitor has a large capacitance and low ESR, the voltage ripple at the load will be small. Then the approximate average battery current required to deliver the above average power with a supercapacitor present is given by the following:

$$i_B(ave) \approx \frac{p_L(ave)}{v_L(ave)} \approx \frac{p_L(ave)}{V_B - \frac{p_L(ave)}{V_B} R_B} \qquad (29)$$

A more accurate expression is the following:

$$i_B(ave) \approx \frac{V_B \pm \sqrt{V_B{}^2 - 4\,p_L(ave) \cdot R_B}}{2R_B} \qquad (30)$$

Note that the current in the above equations depends on the *average* power rather than the peak power drawn in each pulse, resulting in a significant reduction in peak battery current compared to that without a supercapacitor. (This benefit vanishes with very large duty cycles, close to 1.0, as before.)

The average voltage at the output with a high-C, low-ESR supercapacitor connected can be approximated by the following:

$$v_L(ave) \approx V_B - i_B(ave) \cdot R_B \qquad (31)$$

As in the case of a fixed-current load, the voltage drop during the pulse with a supercapacitor present is reduced significantly over that with the battery alone.

With a supercapacitor connected, the approximate load current during a fixed-power pulse is the following:

$$I_{pulse} \approx \frac{p_{pulse}}{v_L(ave)} \qquad (32)$$

The corresponding drop in output voltage under load can again be approximated roughly by the voltage drop when only the supercapacitor supplies the full load current (neglecting the contribution of battery current), as follows:

$$V_{drop} \approx I_{pulse}(R_C - \frac{T_{ON}}{C}) \quad (33)$$

If the source remains connected during the pulse, the voltage drop will be less than the value given by this equation. As in the fixed-current case, it may be desirable to disconnect the source from the load and supercapacitor when the load pulse is applied, if the load is electrically noisy.

When simulating a fixed-power load in Figure 5 with a sample interval equal to Δt, it can be shown that the source (battery) current satisfies the following equation involving the load power, P, and Δt:

$$a_B \cdot {i_B}^2 + b_B \cdot i_B + c_B = 0 \quad (34)$$

where

$$a_B = R_B[R_B(1 + \frac{\Delta t}{2R_C C}) + R_C] \quad (35)$$

$$b_B = v_C R_B(1 + \frac{\Delta t}{R_C C}) - V_B R_B(\frac{\Delta t}{R_C C} + 2) - V_B R_C \quad (36)$$

$$c_B = V_B(V_B - v_C) + PR_C + \frac{\Delta t}{2R_C C}({v_C}^2 - 2v_C V_B + {V_B}^2) \quad (37)$$

The solution to the above is given by the following:

$$i_B = \frac{-b_B \pm \sqrt{{b_B}^2 - 4a_B c_B}}{2a_B} \quad (38)$$

The supercapacitor current may be calculated in terms of i_B from the following equation:

$$i_c = \frac{v_C - (V_B - i_B R_B)}{R_C} \quad (39)$$

If a current limit, I_{Lim}, is specified and if $i_B > I_{Lim}$ in the simulation, then i_B is set equal to $I_{Lim,}$ and i_C is calculated as follows:

$$i_c = \frac{v_C - (V_B - I_{Lim} R_B)}{R_C} \quad (40)$$

Alternatively, the supercapacitor current may be found directly, in the same way i_B was calculated. It can be shown that it satisfies the following equation involving the load power, P:

$$a_C {i_C}^2 + b_C \cdot i_C + c_C = 0 \quad (41)$$

where

$$a_C = R_C(1 + \frac{R_C}{R_B}) + \frac{\Delta t}{2C} \quad (42)$$

$$b_C = \frac{R_C}{R_B}(V_B - 2v_C) - v_C \quad (43)$$

$$c_C = v_C(\frac{v_C - V_B}{R_B}) + P \quad (44)$$

The supercapacitor current i_C is then the solution to the quadratic, as follows:

$$i_C = \frac{-b_C \pm \sqrt{b_C{}^2 - 4a_C c_C}}{2a_C} \quad (45)$$

The change in the supercapacitor's voltage by the end of the time interval (Δt) is then found, using the relationship in equation 17, as follows:

$$\Delta v_C = \frac{i_C \cdot \Delta t}{C} \quad (46)$$

The load voltage may be determined from one of the following equations:

$$v_L = V_B - i_B R_B \quad (47)$$

or

$$v_L = v_C - i_C R_C \quad (48)$$

The above equations are used in the Fixed-Power Pulsed-Load Simulator.

Determination of C and ESR Required

Once the desired circuit configuration (such those shown in Figures 2, 3 and 4) is decided, the values of the capacitance and ESR of the supercapacitor need to be determined. The main criteria that determine these parameters are the following values:

- Minimum battery/source voltage during operation (and maximum voltage, if relevant).
- Maximum permitted source current drawn from host.
- Minimum load voltage required for correct operation of the load.
- Load current/power profile, consisting of pulse period and duty cycle, current/power required during load pulse, and current/power required during intervals between load pulses.
- Maximum permitted ripple in load voltage, if specified.

In many applications, there may be a range of values of C and ESR that will enable the load to function. The less demanding the application is, the wider this range is likely to be. The combinations of values that are acceptable may include high C and high ESR through to low C and low ESR (relatively speaking) and, for the most demanding applications, high C and low ESR. High capacitance minimises the voltage droop during the load pulses, while low ESR minimises the voltage drop at the instant the load pulses are applied.

In some very demanding applications, the current drawn from the source may be too high even with one of the available low-ESR, high-C supercapacitors. If this is the case, but it appears that the requirements could be met with a supercapacitor with even lower ESR or higher C, then it may be possible to meet the specification by another means. This is to increase the source resistance either by using a cheaper MOSFET with increased ON-resistance in the current-limiter circuit, or by adding the right amount of resistance to the power input rail from the source. This additional resistance can help to keep the current drawn from the source during pulses below the maximum value permitted. Care should be taken not to add too much resistance, as this will reduce the average load voltage.

Another solution that is more energy-efficient is to use a current-limit circuit that limits the peak current drawn during operation as well as the charging current during power-up (refer to Reference 1).

Spreadsheets published by CAP-XX for the simulation of fixed-current and fixed-power pulsed loads can be very useful in confirming the minimum C and maximum ESR required in a supercapacitor. (The spreadsheets may be downloaded from the CAP-XX web site.) SPICE modelling is also very useful; a simple linear model of the supercapacitor that uses only ESR and C will generally provide acceptable results in most low-frequency applications.

The calculation of the approximate values of C and ESR required is simpler for fixed-current loads than it is for fixed-power loads, as the equations are simpler. However, it is usually possible to obtain a good estimate of the values in the fixed-power case by approximation. Both techniques are discussed below.

Before attempting to calculate the supercapacitor's parameters, some basic checking should be done to determine whether the source is capable of supplying the load.

Voltage check: If the minimum value of the source voltage is below the minimum at which the load will operate (unless there is a boost converter between the two), then the application is not feasible without boosting the voltage or re-designing the system.

Power check: The supercapacitor acts as a first-order low-pass filter on the power supply. This smooths the load and enables one to use average load current or average power as a reasonable approximation to the current or power that will be drawn from the source. However, if the average power required by the load is more than the average power the source can provide, then the application is not feasible at all. If a DC-DC converter is to be used, then its efficiency must be taken into account in this calculation.

In the case of a *fixed-current* load, the average load current is given by the following:

$$i_{L,Ave} = D \cdot i_{Peak} + (1 - D) i_{Continuous} \qquad (49)$$

(D is the duty cycle, between 0 and 1, and the continuous current is the worst-case expected average current between pulses during normal operation.) This average current must be less than the average current the source is capable of supplying.

In the case of a *fixed-power* load, the average load power is given by the following:

$$p_{L,Ave} = D \cdot p_{Pulse} + (1 - D) p_{Continuous} \qquad (50)$$

This average load power must be less than the minimum average power that the source can supply, which is given by the product of the minimum voltage the source will provide and the maximum average current that may be drawn from it, as follows:

$$p_{B,\min,Ave} = V_{B,\min} \cdot i_{B,\max} \qquad (51)$$

If a DC-DC converter having efficiency η ($0 < \eta < 1$) is between the source and load, then the average load power above must be increased, as follows:

$$p_{L,Ave} = \frac{1}{\eta}(D \cdot p_{Pulse} + (1 - D) p_{Continuous}) \qquad (52)$$

Again, this must not exceed $p_{B,min,Ave}$. If a fixed-current load is driven by a DC-DC converter, then the load current should be converted to load power at the output of the converter, and the input power estimated by dividing by the efficiency; the result can then be compared with the minimum average source power.

C and ESR required for a fixed-current pulsed load in the circuit in Figure 2: To continue, a copy of the fixed-current supercapacitor pulse-simulator spreadsheet from the CAP-XX web site is required. Open the spreadsheet and refer to the documentation worksheet, "Read Me First", for information on what the simulator does and how to use it.
Enter the values in the relevant cells for the source (battery) voltage, source resistance, and pulse width and period. If the current-limiter has significant series resistance, it should be added to the source resistance for the purpose of the simulation. Enter a simulation time somewhere between about one period and 10 periods long; five is a good number. (Simulation time is arbitrary, but it is useful to be able to see more than one period in order to see any trend, and it is not advisable to have too many cycles in the simulation period, as this may result in errors in the simulation resulting from too few simulation steps per pulse.)

If suitable values of C and ESR for the supercapacitor are not known, then initial values may be guessed. For example, values of 20mΩ to 100mΩ and 0.25F to 1.5F (respectively) could be reasonable starting points, depending on the application.

Enter a value for the continuous current drawn by the load; this is the worst-case average current drawn between load pulses. Enter a value for the pulse current; this is the current drawn during the pulses, excluding the continuous current. (The total current drawn during the pulses will be the sum of the continuous current and the pulse current.)

Enter values for the source current limits during pulses and between pulses. The current drawn from the source/battery will be limited to these values during the relevant time intervals. If the current-limiter in Figure 2 operates only while charging the supercapacitor and then permits current of any value to flow, the values of the current limits may be set sufficiently high that there is no limiting action (say a 10A limit for a 2A maximum in a typical GPRS application). The result can then be examined to determine if any specified maximum source current has been exceeded by checking the "Current Limit Exceeded" flag. If the limiter acts during normal operation as well, then the appropriate limits should be entered. There are separate settings for current limits during pulses and between pulses. This is because in some applications the source/battery may be isolated from the load during pulses, to minimise electrical noise in other circuits; this may be simulated by setting the limit during pulses to zero.

Enter a value for the initial open-circuit voltage on the supercapacitor. The most useful value is typically the steady-state voltage that would be measured at the leading edge of one of the pulses if the supercapacitor were open-circuit. This steady-state value is calculated by the spreadsheet and displayed in the cell labelled 'Steady-State Vc'. (This value is correct if no limiting takes place.) If this value is entered as the initial voltage, then the simulation will reflect the circuit's behaviour in its steady state. (There should then be no difference visible between the voltages on the supercapacitor at the leading edges of all pulses displayed on the chart.)

Note: If the initial voltage on the supercapacitor is higher than the steady-state value, then the voltage on the supercapacitor will begin to decay gradually to its steady-state value. If the initial voltage is lower than the steady-state value, then it will gradually increase to that value. Users should be aware that it might take a long time to reach the steady state, even though the load voltage for the duration of the simulation may not appear to be changing very much. If limiting takes place, then the calculated value of 'Steady-State Vc' will be incorrect. In this case, the user should iterate to a solution by reading the value of 'Vinit Supercap' from the last pulse in the simulation (shown as Vc(tx) in Figure 6) and using this as the new value of 'Vinit Supercap' in the table of entries (i.e., the value used for the first pulse). Repeat this process until the value of Vinit supercap read from the simulation graph for the last pulse is approximately the same as the value for the first pulse.

After all the above values have been entered, the simulation will update itself to display the result. It is then possible to examine the load voltage and determine whether it remains within the range in which the load will function. The source current may also be checked to determine whether it

exceeds the maximum value allowed. If the ESR of the supercapacitor is too high, the initial voltage drop at the onset of each load pulse may be too great. If the capacitance is too low, the voltage droop during the pulses may be too large. If there is a wide margin in the load voltage level, then it may be possible to relax the ESR and/or capacitance values used in the simulation.

Examples from Pulse Simulator and Actual Waveforms

Example 1: PC Card transmitting class 10 GPRS with no current limit during operation.

A GPRS transmitter is to operate in class 10 mode on a 3.3V PC card. A class 10 GPRS pulse is 1.154ms wide, with a period of 4.616ms. After initialisation, the card draws 100mA between pulses, and the peak current is 2.0A during transmission. The maximum current permitted by the PC Card specification is 1A. The source resistance is 150mΩ and the series resistance of the current-limiter plus circuit traces is 50mΩ, giving a total simulated "source" resistance of 200mΩ. The current-limiter acts during charging of the supercapacitor only, and subsequently turns on fully. We wish to find the capacitance and ESR of a supercapacitor that will enable this application to work without the load voltage dropping below 3.0V or the source current exceeding 1A.

Parameters to enter in the SupercapPulseSimulatorFixedCurrent:

V Source:	3.3V	
Source $R_{(int)}$:	0.2Ω	
V_{init} Supercap	Set = Steady-State Vc	
Supercap C:	0.1F	{Initial trial value}
Supercap ESR:	100mΩ	{Initial trial value}
Pulse Width:	1.154ms	{Can be entered as =4*0.577 to avoid computation}
Pulse Period:	4.616ms	{Can be entered as =8*0.577 to avoid computation}
Continuous Current:	0.1A	{ = average current between transmitted pulses}
Pulse Current (excl. cont.):	1.9A	{Current during pulses = Continuous Current + Pulse Current}
Source I_{lim} (during pulses):	10A	{Current limit during pulses; set to high value for no limiting}
Source I_{lim} (betw. pulses):	10A	{Current limit between pulses, set to high value for no limiting}
Simulation Time:	0.02308s	{5 x Pulse period is a good value for seeing what happens; can be entered as =5*Pulse Period/1000 to avoid computation}

The initial C & ESR values chosen were those of a CAP-XX supercapacitor, GS212. This 1.55mm device is the thinnest of the GS2 range. The GS footprint is designed to fit across a PC Card. The resultant graph (Fixed I (V and I vs t) chart of the simulator) is shown in Figure 7, below. The minimum output voltage is 3.09V, which is greater than the 3.0V minimum allowed, but the maximum source current, i_B = 1.07A, is just over the 1.0A maximum constraint. A supercapacitor with a slightly lower ESR and/or higher C is needed. Choosing the next thicker GS2 supercapacitor, GW209 (2.06mm), which has a slightly lower ESR and higher C meets all requirements.

Figure 8 is the output from the Fixed-Current Pulse Simulator with a CAP-XX supercapacitor, GW209. The parameters are as above, except the following:

Supercap C:	0.12F
Supercap ESR:	90mΩ

Figure 9 is the actual output from a test on a system with the above characteristics. Note that the two responses are very similar. The table below compares predicted values from the simulator and actual values measured on a test circuit.

	Simulator Values	Measured Values
Peak Current	**0.98A**	**0.94A**
Minimum output voltage	**3.058V**	**3.04V**

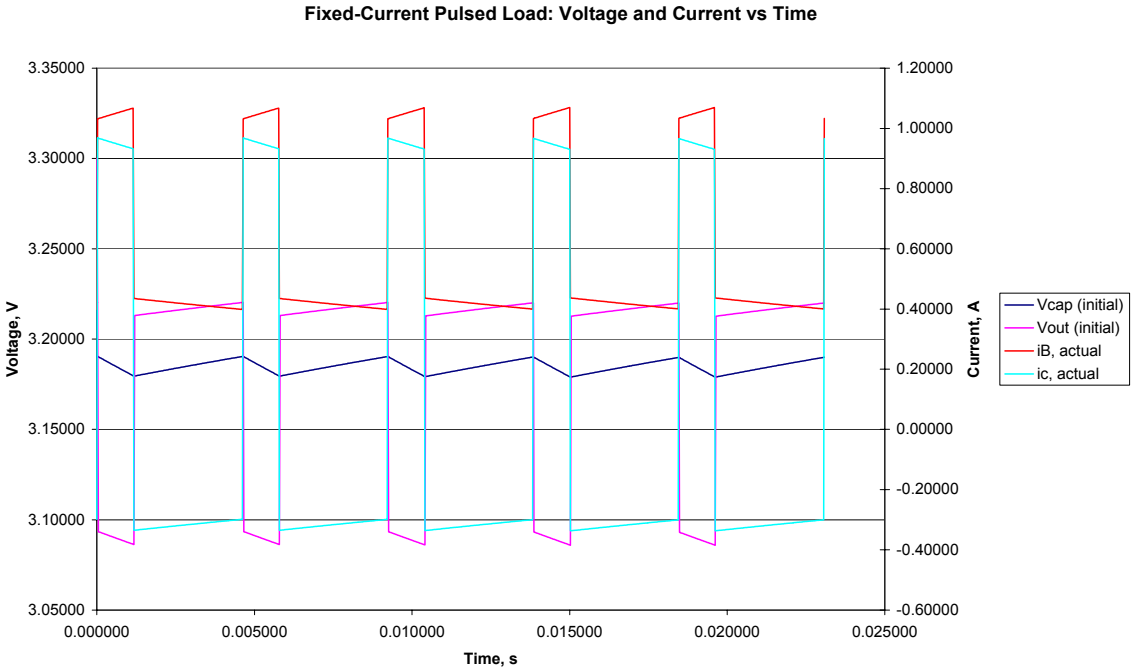

Figure 7 Fixed-Current Pulsed-Load Simulation of Class 10 PC Card With GW212 CAP-XX Supercapacitor

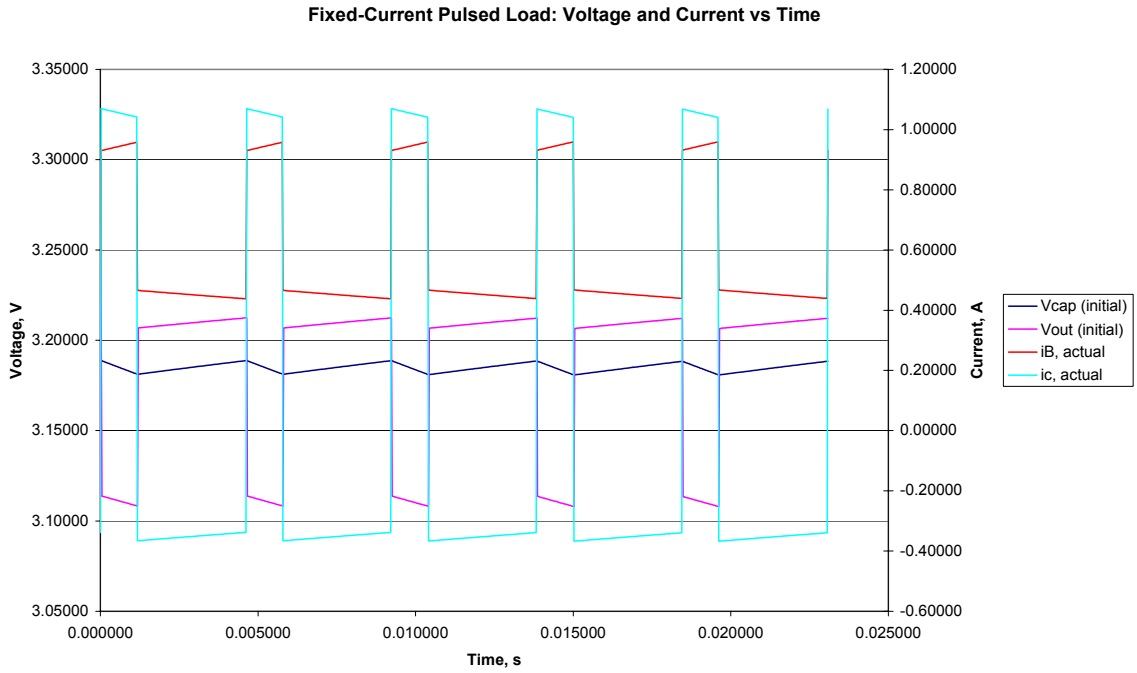

Figure 8 Fixed-Current Pulsed-Load Simulation of GPRS Class 10 PC Card With GW209 CAP-XX Supercapacitor

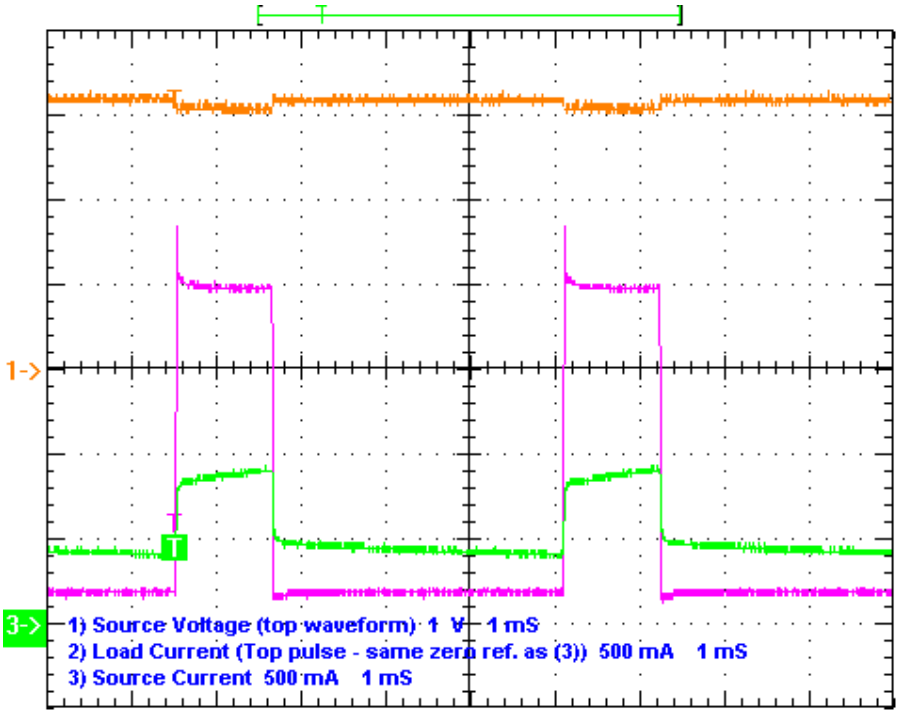

Figure 9 Voltage and Current Waveforms from PC Card System Using GW209 Supercapacitor with GPRS Class 10 Pulsed Load

Example 2: CF+ Card transmitting class 8 GPRS with no current limit during operation.

A GPRS transmitter is to operate in class 8 mode on a 3.3V CF+ card. A class 8 GPRS pulse is 577μS wide, with a period of 4.616ms. After initialisation, the card draws 100mA between pulses, and the peak current is 1.8A during transmission. The maximum current permitted by the CF+ Card specification is 500mA in Power Level 1. The source resistance is 180mΩ and the series resistance of the current-limiter plus circuit traces is 70mΩ, giving a total simulated "source" resistance of 250mΩ. The current-limiter acts during charging of the supercapacitor only, and subsequently turns on fully. We wish to find the C and ESR of a supercapacitor that will enable this application to work without the load voltage dropping below 3.0V or the source current exceeding 0.5A.

Parameters to enter in the SupercapPulseSimulatorFixedCurrent:

V Source:	3.3V	
Source $R_{(int)}$:	0.25Ω	
V_{init} Supercap	Set = Steady-State Vc	
Supercap C:	0.09F	{Initial trial value}
Supercap ESR:	115mΩ	{Iinitial trial value}
Pulse Width:	0.577ms	{Can be entered as =*0.577 to avoid computation}
Pulse Period:	4.616ms	{Can be entered as =8*0.577 to avoid computation}
Continuous Current:	0.1A	{ = average current between transmitted pulses}
Pulse Current (excl. cont.):	1.7A	{Current during pulses = Continuous Current + Pulse Current}
Source I_{lim} (during pulses):	10A	{Current limit during pulses; set to high value for no limiting}
Source I_{lim} (betw. pulses):	10A	{Current limit between pulses; set to high value for no limiting}
Simulation Time:	0.02308s	{5 x Pulse period is a good value for seeing what happens; can be entered as =5*Pulse Period/1000 to avoid computation}

The initial C & ESR chosen were the values applicable to a CAP-XX device, GW214. This 1.7mm device is the thinnest of the GW2 range. The GW range has a smaller footprint than the GS range and is suitable for CF cards. The maximum source current for this solution, i_B = 0.87A, is well over the 0.5A max current constraint. A supercapacitor with a much lower ESR and/or higher C is needed. Choosing the lowest-ESR GW2 supercapacitor (GW208: 40mΩ, 0.3F) results in a maximum source current of 0.52A and a minimum output voltage of 3.16V. This nearly meets all requirements. As mentioned previously in *Determination of C and ESR Required*, a technique that can be used to reduce the source current is to increase the source resistance. This can be done by using a lower-cost MOSFET with a higher $R_{DS(ON)}$, or by increasing the sense resistor if using the continuous current-limiting circuit in Reference 1, or by inserting a small resistor between the power source and the supercapacitor. In the above example, we now increase the source resistance by 50mΩ to 300mΩ.

Figure 10 is the output from the Fixed-Current Pulse Simulator with a GW208 and a source resistance of 300mΩ. Parameters are as above, except the following:

Source R(int): 0.3Ω
Supercap C: 0.3F
Supercap ESR: 40mΩ

Figure 11 is the actual output from a test on a system with the above characteristics. Note that the two responses are very similar. The table below compares predicted values from the simulator and actual values measured on a test circuit.

	Simulator Values	Measured Values
Peak Current	**0.49A**	**0.47A**
Minimum output voltage	**3.15V**	**3.16V**

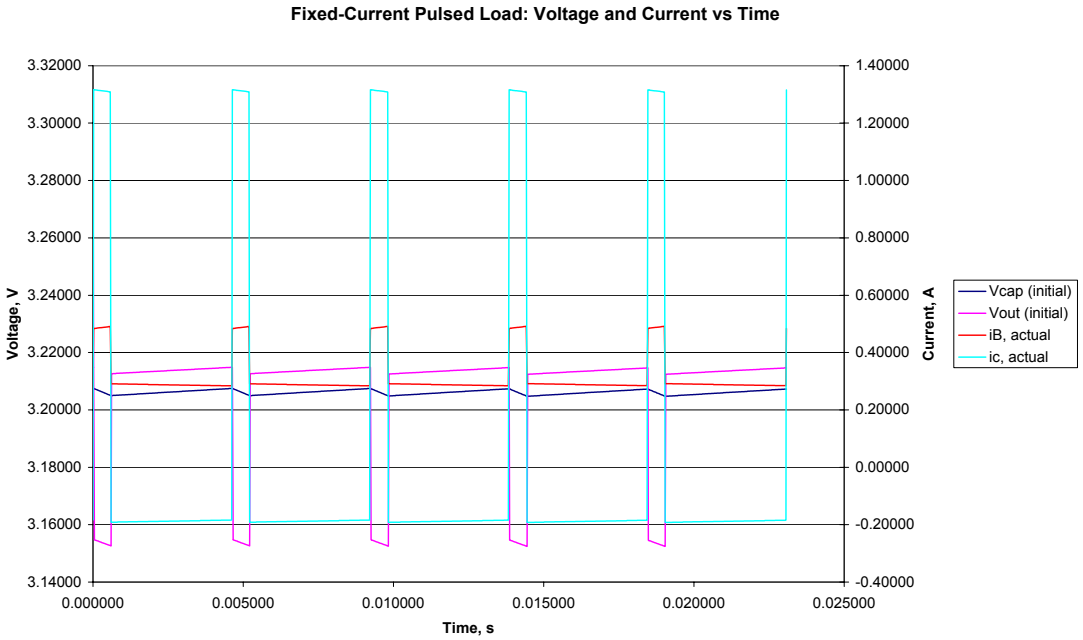

Figure 10 Fixed-Current Pulsed-Load Simulation of GPRS Class 8 CF+ Card with GW208 CAP-XX Supercapacitor

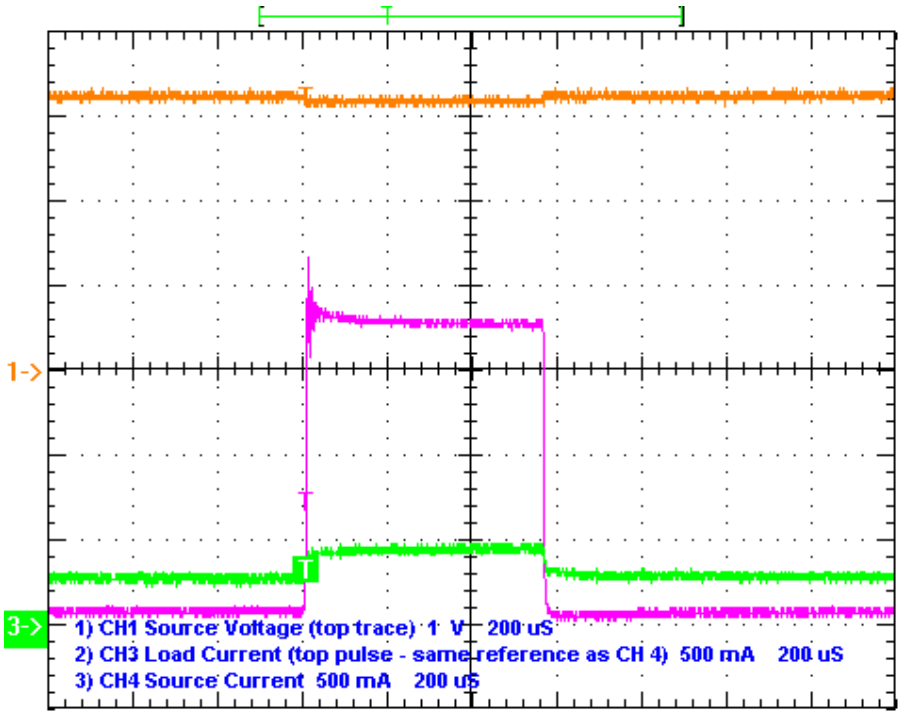

Figure 11 Voltage and Current Waveforms from CF+ Card System Using GW208 Supercapacitor with GPRS Class 8 Pulsed Load

C and ESR required for a fixed-current pulsed load in the circuit in Figure 3: During periods when the current-limiter supplies power to the load (and the DC-DC converter is inactive), the circuit behaves in the same way as that of Figure 2, which is discussed above. If the supply voltage and the required load voltage are different, the DC-DC converter will be in use, which modifies the circuit's behaviour.

The simulator spreadsheet is not designed to simulate the circuit of Figure 3 with the DC-DC converter in operation, but it can assist in determining the overall behaviour. To simulate this case, it is necessary first to treat the output of the DC-DC converter as if it is the source, with the source current-limit values in the simulation set appropriately to that of the converter. (The output of the DC-DC converter must be able to limit the current, or there must be a limiter on its output, in order to maximise the benefit of the supercapacitor and limit the current drawn from the source.) The circuit is then simulated as described above, using a source resistance that is a good approximation of that of the DC-DC converter plus any trace resistances between the converter and the supercapacitor, plus the resistance of a separate current-limiter, if there is one.

Next, it is necessary to know the efficiency of the DC-DC converter. By examining the simulation result, the load voltage and "source" current are determined, where this "source" is the output of the DC-DC converter. From these values, the maximum power drawn from the actual source can be estimated, provided the DC-DC converter has a rapid response in transferring the load to the source. If the efficiency of the DC-DC converter is known, the following steps may be used to calculate the power and current drawn from the source:

- Make sure that the spreadsheet is simulating the steady-state condition, so that the voltage on the supercapacitor is correct. This may be done by comparing the "open-circuit" voltages on the supercapacitor at the leading edges of pulses early in the simulation and at the end of the simulation. They should agree closely (preferably to four significant figures or better). If the system being simulated has not yet reached steady-state, then the last value can be entered as

the starting value of supercapacitor voltage for another simulation, and so on, in iterative fashion until the system has reached its steady state.

- Examine the simulation results in the spreadsheet and find the load voltage, v_O, at the moment the DC-DC converter ("source") goes into current-limiting. At this moment, the power output by the DC-DC converter is expected to be at (or close to) its highest value. Find the power output from the following equation:

$$p = v_O \cdot i_{\max} \tag{53}$$

- If, as discussed above, increases in load are transferred rapidly to the input, then the maximum input power can be estimated from its efficiency, as follows:

$$p_{in} = \frac{p}{\eta} \tag{54}$$

- The input current can then be calculated, as follows, using the same formula as in equation 27:

$$i_B = \frac{V_B \pm \sqrt{V_B{}^2 - 4 p_{in} R_B}}{2R_B} \tag{55}$$

If the input current exceeds the maximum value in the relevant specification, then the simulated supercapacitor's capacitance may be increased and/or its ESR may be reduced to determine if this will bring the input current within specification. If the input current is much lower than the allowed value, it may be possible to reduce the capacitance and/or increase its ESR.

If the voltage ripple on the load is too large, the capacitance may be increased and/or its ESR reduced, and vice versa, if the ripple voltage is too far under the required value, provided the source current requirement is also met.

C and ESR required for a fixed-current or fixed-power pulsed load in the circuit in Figure 4: In this circuit configuration, the DC-DC converter's purpose is to maintain a stable voltage to the load, so we assume that its output voltage does not change during the load pulse. The power and voltage to the load have the simple relationship $p_L = v_L i_L$. If we can again assume the DC-DC converter transfers its load rapidly to its input, we can calculate the load the converter presents at its input. This is expected to behave as a fixed-power load, to a good approximation. Equation 54 above gives the relationship between the power at the converter's output, its efficiency and the input power.

Using the figures obtained above for the power drawn by the DC-DC converter during load pulses and between load pulses, the system reduces to the case of Figure 2 with a fixed-power load, which is discussed below.

The advantages of the circuit in Figure 4 are not only the stability of the output voltage, but also that the voltage on the supercapacitor can be allowed to change by a relatively large amount without affecting the load. This makes more effective use of the energy-storage capacity of the supercapacitor than is the case when it is connected in parallel with the load.

C and ESR required for a fixed-power pulsed load in the circuit in Figure 2: To continue, a copy of the fixed-power supercapacitor pulse-simulator spreadsheet from the CAP-XX web site is required. Open the spreadsheet and refer to the documentation worksheet, "Read Me First", for information on what the simulator does and how to use it.

Enter suitable values in the relevant cells for the source (battery) voltage, source resistance and pulse width and period. If the current-limiter has significant series resistance, it should be added to

the source resistance for the purpose of the simulation. Enter a simulation time somewhere between about one period and 10 periods long. (As before, simulation time is arbitrary, but it is useful to be able to see more than one period in order to see any trend, and it is not advisable to have too many cycles in the simulation period, as this may result in errors in the simulation resulting from too few simulation steps per pulse.)

If suitable values of C and ESR for the supercapacitor are not known, then initial values may be guessed. For example, values of 0.25F to 1.5F and 20mΩ to 100mΩ (respectively) could be reasonable starting points, depending on the application.

Enter a value for the continuous power drawn by the load; this is the power drawn between load pulses. Enter a value for the pulse power; this is the power drawn during the pulses, excluding the continuous power. (The total power drawn during the pulses will be the sum of the continuous power and the pulse power.)

As in the fixed-current pulse simulator, enter values for the source current limits during pulses and between pulses. The current drawn from the source/battery will be limited to these values during the relevant time intervals. If the current-limiter in Figure 2 operates only while charging the supercapacitor and then permits current of any value to flow, the values of the current limits may be set sufficiently high that there is no limiting action. The result can then be examined to determine if any specified maximum source current has been exceeded. If the limiter acts during normal operation as well, then the appropriate limits should be entered. In some applications, the source/battery may be isolated from the load during pulses, to minimise electrical noise in other circuits; this may be simulated by setting the limit during pulses to zero.

Enter a value for the initial open-circuit voltage on the supercapacitor. The most useful value is typically the steady-state voltage that would be measured at the leading edge of one of the pulses if the supercapacitor were open-circuit. This steady-state value is calculated by the spreadsheet and displayed in one of the lower cells of non-editable values. (This value is correct if no limiting takes place.) If this value is entered as the initial voltage, then the simulation will reflect the circuit's behaviour in steady state. (There should then be no difference visible between the voltages on the supercapacitor at the leading edges of all pulses displayed on the chart.)

Note: If the initial voltage on the supercapacitor is higher than the steady-state value, then the voltage on the supercapacitor will begin to decay gradually to its steady-state value. If the initial voltage is lower than the steady-state value, then it will gradually increase to that value. Users should be aware that it might take a long time to reach the steady state, even though the load voltage for the duration of the simulation may not appear to be changing very much.

After all the above values have been entered, the simulation will update itself to display the result. It is then possible to examine the load voltage and determine whether it remains within the range in which the real load will function. The source current may also be checked to determine whether it exceeds the maximum value required. If the ESR of the supercapacitor is too high, the initial voltage drop at the onset of each load pulse may be too much. If the capacitance is too low, the voltage droop during the pulses may be too large. If there is a wide margin in the voltage level, then it may be possible to relax the ESR and/or capacitance used in the simulation.

Example 3: PC Card transmitting class 10 GPRS with no current limit during operation.

A supercapacitor is required that will enable a 3.3V PC Card (PCMCIA) GPRS device to operate in class 10 mode. After initialisation, the load draws 0.33W (approximately 0.1A) continuously and 5.9W in addition to this during the pulses. The voltage must not drop below 3.0V during transmissions. The source resistance is 0.2Ω, and the current-limiter's series resistance plus the trace resistance is 70mΩ. A class 10 transmission pulse is 1.154ms long, with a period of 4.616ms.

For a 3.3V device, the PC Card specification allows the card to draw a peak current of up to 1A (averaged over any 10ms period) and an average current of 750mA (averaged over any 1s period).

The following parameters should be entered into the user-editable cells of the SupercapPulseSimulatorFixedPower:

V Source:	3.3V	
Source $R_{(int)}$:	0.27Ω	
V_{init} Supercap	3.25V	{Choose an initial value slightly less than Vsource}
Supercap C:	0.16F	{Initial trial value GS202}
Supercap ESR:	70mΩ	{Initial trial value GS202}
Pulse Width:	1.154ms	{Can be entered as =4*0.577 to avoid computation}
Pulse Period:	4.616ms	{Can be entered as =8*0.577 to avoid computation}
Continuous Power:	0.33W	{ = average power between transmit pulses}
Pulse Power (excl. cont.):	5.9W	{Power during pulses = Continuous Power + Pulse Power}
Source I_{lim} (during pulses):	10A	{Current limit during pulses; set to high value for no limiting}
Source I_{lim} (betw. pulses):	10A	{Current limit between pulses; set to high value for no limiting}
Simulation Time:	0.02308s	{5 x Pulse period is a good value for seeing what happens; can be entered as =5*Pulse Period/1000 to avoid computation}

The initial supercapacitor voltage is determined by iteration, as described above. Then, each time C or ESR (or any other key parameter) is changed, the initial supercapacitor voltage should again be updated so that the system is in its steady state, as described above.

It is found that a CAP-XX GS204 supercapacitor with C=0.25F and ESR=40mΩ and V_{init} Supercap = 3.143V gives the simulation result shown in the chart below. The load (output) voltage remains above 3.0V, and the source current does not exceed the specified values. The load power (not shown) is a rectangular wave, as specified.

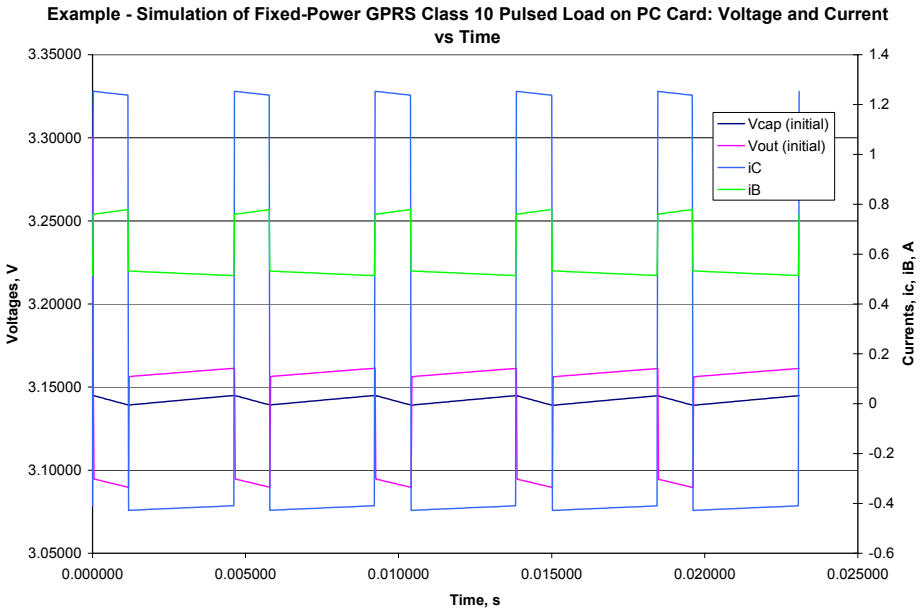

Figure 12 Fixed-Power Pulsed-Load Simulation of GPRS Class 10 PC Card with a GS204 Supercapacitor with No Current Limit

Other CAP-XX supercapacitors may also be used to meet the specification. For example, a GS205 (0.45F, 24mΩ) will work well, as will a GS207 (0.95F, 28mΩ), a GS208 (1.4F, 20mΩ), a GW208 (0.3F, 40mΩ), a GW210 (0.35F, 32mΩ) and a GW211 (0.8F, 34mΩ). The thicknesses of some devices may be factors in determining whether they are appropriate for the design.

C and ESR required for a fixed-power pulsed load in the circuit in Figure 3: During periods when the current-limiter supplies power to the load (and the DC-DC converter is inactive), the circuit behaves in the same way as that of Figure 2, which is discussed above. If the supply voltage and the required load voltage are different, the DC-DC converter will be in use, modifying the circuit's behaviour.

As mentioned in the fixed-current case, the simulator spreadsheet is not designed to simulate the circuit of Figure 3 with the DC-DC converter in operation, but it can assist in determining the overall behaviour. To simulate this configuration, it is necessary first to treat the output of the DC-DC converter as if it is the source, with the source current-limit values in the simulation set appropriately to that of the converter. (The output of the DC-DC converter must be able to limit the current, or there must be a limiter on its output, in order to maximise the benefit of the supercapacitor and limit the current drawn from the source.) The circuit is then simulated as described above, using a source resistance that is a good approximation of that of the DC-DC converter plus any trace resistances between the converter and the supercapacitor, plus the resistance of a separate current-limiter, if there is one.

Next, it is necessary to know the efficiency of the DC-DC converter. By examining the simulation result, the load voltage and "source" current are determined, where this "source" is the output of the DC-DC converter. From these values, the maximum power drawn from the actual source can be estimated, provided the DC-DC converter has a rapid response in transferring the load to the source. If the efficiency of the DC-DC converter is known, the following steps may be used to calculate the power and current drawn from the source:

- Make sure that the spreadsheet is simulating the steady-state condition, so that the voltage on the supercapacitor is correct. This may be done by comparing the "open-circuit" voltages on the supercapacitor at the leading edges of pulses early in the simulation and at the end of the simulation. They should agree closely (preferably to four significant figures or better). If the system being simulated has not yet reached steady-state, then the last value can be entered as the starting value of supercapacitor voltage for another simulation, and so on, in iterative fashion, until the system has reached its steady state.
- Examine the simulation results in the spreadsheet. At several points during a pulse, calculate the power drawn from the "source", which is the product $v_L i_B$. Find the maximum value of this power.
- If, as discussed above, increases in load are transferred rapidly to the input, then the maximum DC-DC converter input power can be estimated from its efficiency, as in equation 54, above.
- The input current can then be calculated, using equation 55, above.

If the input current exceeds the maximum value in the relevant specification, then the simulated supercapacitor's capacitance may be increased and/or its ESR may be reduced to determine if this will bring the input current within specification. If the input current is much lower than the allowed value, it may be possible to reduce the capacitance and/or increase its ESR. Some allowance should be made for operating conditions, such as low temperature (which affects C and ESR) and aging of the supercapacitor. (See the data sheet for the relevant device.)

If the voltage ripple on the load is too large, the capacitance may be increased and/or its ESR reduced, and vice versa if the ripple voltage is too far under the required value, provided the source current requirement is also met.

Example 4: PC Card transmitting class 10 GPRS using DC-DC converter with output current limit.

Using the configuration of Figure 3, with a fixed-power pulsed load and current-limited output on the DC-DC converter, we wish to find the values of C and ESR of a supercapacitor that will work, as well as the current-limit value to use on the output of the DC-DC converter. The continuous power drawn by the load is 0.33W and the peak power is an additional 6W (total 6.33W during pulses). The load pulses are class 10 GPRS pulses, which have a duration of 1.154ms and a period of 4.616ms. The source voltage supplying the DC-DC converter is 3.3V, its source resistance is 200mΩ, the output voltage of the DC-DC converter is 4.3V, and the output resistance of the converter is 10mΩ. The efficiency of the converter is 90%.

It can be shown by trial-and-error that several different supercapacitors may be used in this application. One such device is a GW206, which has C = 0.35F and ESR = R_C = 45mΩ. The above values are entered in the fixed-power worksheet of the pulsed-load simulator spreadsheet. Note that the DC-DC converter's output is considered the output of the source in the spreadsheet initially, so that its peak power output may be determined.

Next, a value must be selected for the current limit at the output of the DC-DC converter. Again using trial-and-error, it was found that 0.65A was suitable, while the steady-state initial open-circuit voltage on the supercapacitor is 4.285V. Then the peak power output from the DC-DC converter can be found by examining the values of the output current and voltage in the simulation and multiplying them to find the power at any instant. The maximum value is 2.785W. The corresponding input power to the DC-DC converter is therefore 2.785/0.9 W = 3.095W. Solving the quadratic equation (using Equation 55) for the input current to the DC-DC converter with this power (using V_B = 3.3V and R_B = 200mΩ), we find the maximum input current delivered by the source is 1.0A. This is below the value allowed by the PC Card specification, as the specification allows the *average* peak current over any 10ms period to be 1.0A, and this pulse is not continuous.

The following parameters were entered into the SupercapPulseSimulatorFixedPower:

V Source:	4.3V	
Source R(int):	0.01Ω	
V_{init} Supercap:	4.285V	
Supercap C:	0.35F	
Supercap ESR:	45mΩ	
Pulse Width:	1.154ms	{Can be entered as =4*0.577 to avoid computation}
Pulse Period:	4.616ms	{ Can be entered as =8*0.577 to avoid computation}
Continuous Power:	0.33W	{ = average power between transmit pulses}
Pulse Power (excl. cont.):	6.0W	{Power during pulses = Continuous Power + Pulse Power}
Source I_{lim} (during pulses):	0.65A	{Current limit during pulses = 0.65A}
Source I_{lim} (betw. pulses):	0.65A	{Current limit between pulses = 0.65A}
Simulation Time:	0.02308s	{5 x Pulse period is a good value for seeing what happens; can be entered as =5*Pulse Period/1000 to avoid computation}

The graph below is the result of a simulation of the above example.

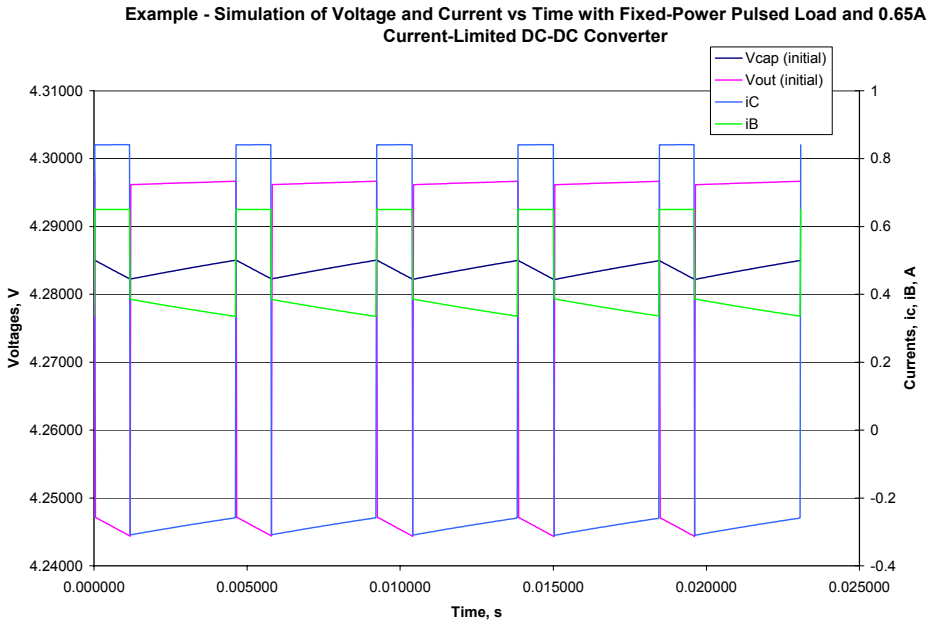

Figure 13 Fixed-Power Pulsed-Load Simulation of GPRS Class 10 PC Card with a GW206 Supercapacitor and 0.65A Current Limit

Several other CAP-XX supercapacitors may be used to meet the requirements of the example. The designer may choose to select the device that results in an optimum ripple voltage, for example, or that meets size requirements. The ripple voltage at the output in the above example is approximately 56mV (simulated), even though the DC-DC converter limits its current output. Lower ripple may be obtained with a supercapacitor having a lower ESR, but if ripple voltage is not important, then a smaller supercapacitor may be preferred.

Conclusion

This Application Note shows how high-power pulsed loads that exceed the maximum current that can be delivered by a CompactFlash or PC Card host can be supported with the aid of a CAP-XX supercapacitor.

It describes the simple equivalent circuits that may be used to represent hosts that power CompactFlash and PC Card devices. It discusses their limitations in the amount of instantaneous current (and power) they can deliver to pulsed loads, and how a supercapacitor solution may be used to solve this problem.

The detailed theory governing the currents and voltages in the load and supercapacitor circuits presented in this Application Note may be used to determine approximate or exact voltage and current waveforms in the circuits. These may be used with any pulsed loads, not just GPRS and GSM waveforms.

The use of a high-capacity, low-ESR supercapacitor often requires that a simple current-limiting circuit be used to prevent the load device from shutting down or overloading the host. Various configurations of such circuits and their controllers may be used to meet the relevant specifications.

Some techniques for selecting the capacitance and ESR of the supercapacitor are presented. A CAP-XX simulation tool (in spreadsheet form) may be used as an aid in selecting the device parameters and to verify that the circuit will function as intended without violating the CompactFlash

or PC Card specification. Examples illustrate how a relatively simple supercapacitor solution permits a high-current pulsed load to operate normally when powered by a low-current source.

Further Information

CAP-XX will be pleased to provide further information on the applications described here, and on the use of supercapacitors in any application. Please use the contact details at the foot of the page, or visit the CAP-XX web site.

This Application Note is available on the CAP-XX web site. On the same web page may be found a downloadable copy of a spreadsheet containing the equations used to calculate the component values, above.

References

1. CAP-XX Application Note 1002, *Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices*; see also the companion spreadsheet to this application note.
2. CAP-XX Application Brief 1009, *Powering GPRS Class 10 Devices on PCMCIA Cards with CAP-XX Supercapacitors*.
3. CAP-XX Application Brief, 1010, *Powering GPRS/GSM Devices on CompactFlash Cards with CAP-XX Supercapacitors.*
4. CAP-XX Application Note 1001, *Current-Limit and Low-Voltage Lockout Circuit for Portable Devices.*

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Appendix E

Application Note 1002

Start-Up Current Limiters for Supercapacitors in PDAs and Other Portable Devices

CAP-XX APPLICATION NOTE No. 1002

Start-Up Current-Limiters for Supercapacitors in PDAs and Other Portable Devices

Revision 2.1, February 2002

Outline

Supercapacitors with low ESR (Equivalent Series Resistance) and high capacitance are ideal components for use in pulsed-power applications, such as GSM and GPRS transmitters, in which the load draws large pulses of current. When connected across the supply, they provide much of the energy needed by each load pulse, reducing voltage ripple and instantaneous supply current. However, they draw a high charging current when the device is turned on. This can cause a battery to shut down, or the supply voltage in a host device to drop because of overloading. This application note describes current-limiting circuits that operate on power-up and/or during operation, allowing the supercapacitor to charge without overloading the supply.

The Problem

Portable devices, such as PDAs and hand-held bar-code scanners, are shrinking in size with each new design. Devices designed to fit into host devices, like PC-Card and Compact Flash devices, must fit into very small spaces and still be able to operate from a power supply that can deliver limited current and power. This makes designing these devices difficult, as GSM and GPRS transmissions (and other applications) require bursts of high power that the supply may not be capable of providing.

A solution to the power problem is to use a CAP-XX supercapacitor with high capacitance and low ESR on the power rail. The low ESR enables the supercapacitor to deliver high power (with only a small voltage drop at the beginning of the peaks), while the high capacitance stores sufficient energy to power the load during the load pulses without a significant voltage droop. The supercapacitor is re-charged between load pulses. However, the large capacitance may introduce a new problem, which is the high charging current it requires on power-up. If the system is being powered by a battery, the high current may blow a fuse or cause the battery to shut down. If the power source is a host's power rail, the specification may prohibit the subsystem from drawing more than a certain amount of current.

How can the power-up charging current be limited to a safe value without compromising operation of the system?

The CAP-XX Solution

A solution to the start-up current problem is to limit it to a safe, known value until the supercapacitor is charged. This Application Note describes circuits that are designed to do this. The MOSFET switch in two of the designs stays on after the initial charging current has stopped flowing, with the result that they will not limit the current during normal operation. The third can be used in a mode that limits the current at any time, which prevents high currents if the system is disconnected from its host and then re-connected while the supercapacitor is still partially charged. During operation, the third solution limits the current based on its actual value, instead of relying only on the low supercapacitor ESR relative to the source impedance. A companion spreadsheet that solves the equations listed below may be found on the same CAP-XX web page from which this document may be downloaded.

Circuit Operation

Introduction

The first two circuits described here are designed to limit the current delivered to the supercapacitor when the power is first applied to the circuit, so that the supercapacitor charges without imposing a high current load on the supply. For applications in which the supercapacitor may remain charged after disconnection from the supply and then be connected to a partially-discharged battery or a lower-voltage power rail, some additional circuitry (not included here) may be required to prevent current flow back from the supercapacitor to the battery/supply.

The first design discussed (see example in Figure 1) uses a series resistor to limit the initial charging current. This is simpler and may cost less than the second circuit, but has the disadvantage that the charging current decreases as the supercapacitor charges up, in a simple exponential way. This means the supercapacitor takes longer to charge than it might from a constant-current source.

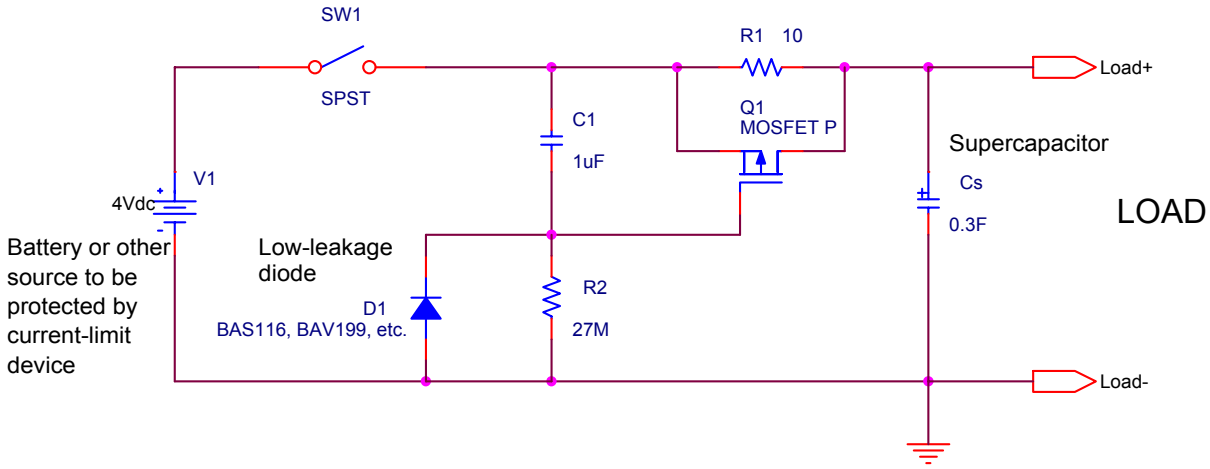

Figure 1 Simple Current-Limiter Circuit Using Series Resistor

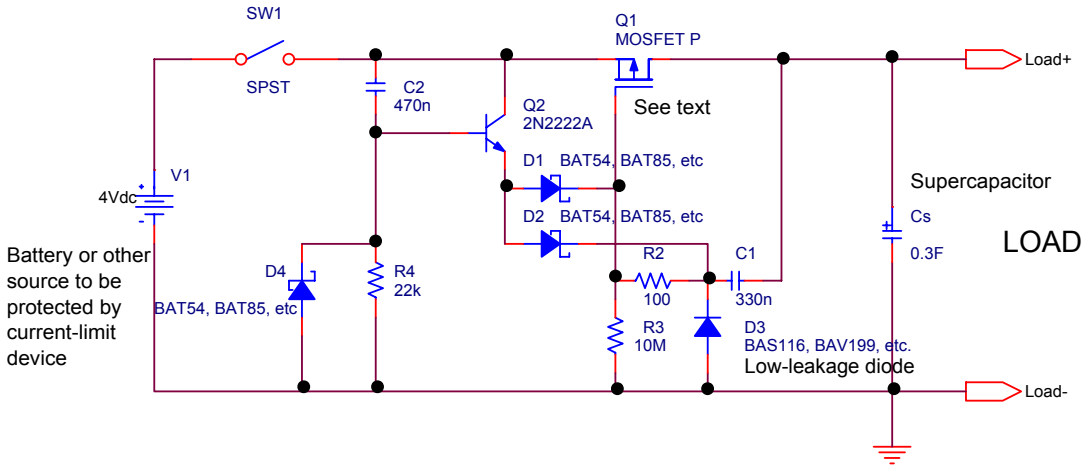

Figure 2 Current-Limiter Circuit Using MOSFET in Constant-Current Design

The second design (see example in Figure 2) uses the MOSFET to charge the supercapacitor in a current-limiting design. The series resistor used in the first design is not required, but some extra circuitry is required to control the gate voltage of the MOSFET. It has the advantage that the supercapacitor takes less time to charge if the same maximum-current criterion is used as in the

circuit of Figure 1. However, the MOSFET selected for Figure 2 must be able to dissipate the heat generated during the charging phase. This is a one-off event each time the device is turned on that typically lasts only a few seconds, so the MOSFET need not be rated to dissipate that amount of power continuously.

The designs shown here are intended to be adapted for operation at various different supply voltages. The lowest supply voltage at which the MOSFET will be able to pass a current without dropping the voltage is determined by its threshold voltage and its output characteristics. To pass a given current, the device should be turned on sufficiently hard to reduce $R_{DS(ON)}$ to a low value. The smaller the threshold voltage, the lower the supply voltage at which the circuit will work successfully and reliably.

An example of a device that should function well at low voltages is IRL5602S, which has a rated gate threshold voltage, $V_{GS(th)}$, of -0.7V to -1.0V. Another is FDR838P, a SuperSOT-8 device, which has a $V_{GS(th)}$ range of -0.4V to -1.5V (typically -0.85V), but a low power rating. The designer should also take into account the supply voltage, maximum load current and power dissipation, etc., in selecting the right MOSFET. Some SuperSOT-8 devices and other small types may be suitable, provided they can dissipate the power during the turn-on charging without becoming too hot. Since it can be difficult to estimate or model the temperature increase of the MOSFET during start-up charging, some experimentation may be required to verify that a device is suitable. After turn-on, the MOSFET should dissipate relatively little power.

Note that, when working with the above circuits, an oscilloscope probe with an impedance of 10MΩ will have a big effect on normal operation if it is connected to the high-value resistors at the MOSFET gates. Only very high input impedance devices (preferably >1GΩ) should ever be connected to these points.

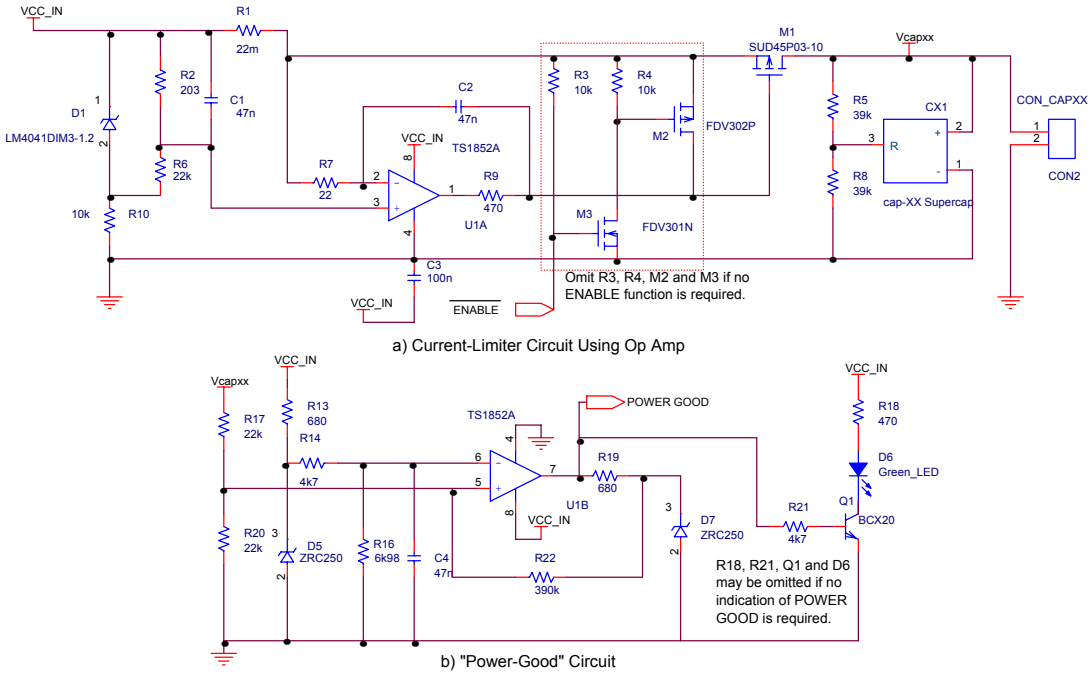

Figure 3 Current-Limiter Circuit Using Operational Amplifier and MOSFET in Constant-Current Feedback Design With Optional ENABLE and POWER GOODCircuits

The third design, Figure 3, measures and controls the current delivered to the supercapacitor by means of an operational amplifier and MOSFET. The component values in the circuit were selected for operation at 3.3V. This circuit avoids the problems associated with high current loads on the

supply (or host) if the device is disconnected from the supply and then re-connected before the supercapacitor has been discharged fully. If enabled, it will limit the current drawn from the supply at any time that the load draws a high current. With the low-cost operational amplifiers used, the response speed is good enough to protect the source on start-up and if there is a sustained high load, but note that it may not be fast enough to respond during a short-duration load pulse.

The circuit in Figure 3(a) is ideal for PC Card and CF Card applications when the designer wishes to make sure that the design complies with the specification, rather than relying on the source impedance of the host device and the ESR of the supercapacitor to limit the current. Relying on the source impedance of the host is particularly problematic, as there is a wide variation in this value between products. The designer need only ensure that the circuit with the current-limiter operating will still provide adequate current for the load. In this regard, the designer is referred to CAP-XX Application Note 1003 and the calculation/simulation aids available on the CAP-XX web site: SupercapPulseSimulatorFixedCurrent.xls and SupercapPulseSimulatorFixedPower.xls.

The portion of Figure 3(a) enclosed in the dotted rectangle is an optional “enable” circuit. If an “enable/disable” function is not required, these components may be omitted.

Also shown (Figure 3(b)) is a circuit that generates a POWER GOOD output when the voltage on the supercapacitor has reached a desired value. This circuit is optional and may be used with any of the current-limiter circuits presented.

Simple Series Resistor Design

Refer to Figure 1. The main current-limiting element in this circuit is the series resistor, R_1. This circuit is designed so that when SW_1 is closed, the supercapacitor is charged via R_1 until its voltage is nearly equal to the supply voltage. In this example, R_1 was selected to give a peak current of 400mA with a 4V supply. C_1 is initially discharged, which ensures that the MOSFET is off. C_1 then charges up via R_2 and turns on the MOSFET later. Refer to Figure 4 for the charging waveforms over the first few seconds. Note that the lowest waveform on the right is the supply current (100mA/div). The moment when the MOSFET turns on can clearly be seen where the current increases briefly, before again falling as the supercapacitor reaches the supply voltage.

The values of R_2 and C_1 are selected to allow enough charging time so that the increased current when the MOSFET comes on is well under the design limit. The moment of turn-on will vary with the threshold voltage of the MOSFET, so some allowance should be made in the timing for variations in component characteristics between devices and with temperature. C_1 may be a lower value than that shown, with an appropriate higher value of R_2. However, C_1 should be high enough to swamp the value of the MOSFET’s gate input capacitance, so that the timing is not affected by variations in MOSFET characteristics. The value used here, 1µF, would be more than sufficient in most circumstances; as a guide, C_1 should be more than 10 times the input capacitance of the MOSFET, and 100 times or more should be suitable in most cases. D_1 should be a device with low reverse current, so it does not affect the charging of C_1.

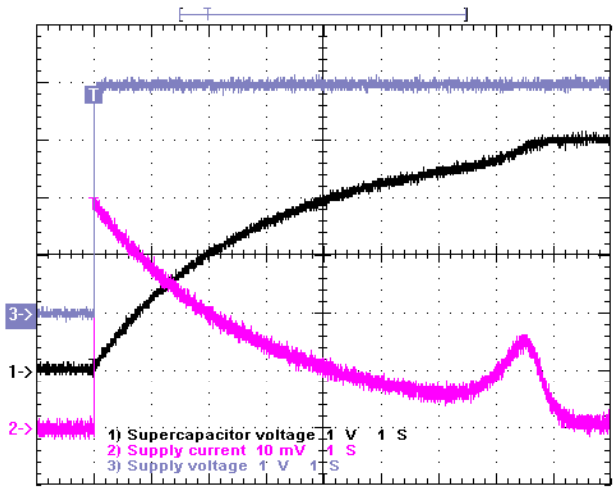

Figure 4 Current (100mA/div) and Voltage Waveforms (1s/div) for Example in Figure 1 (using high reverse-current diode as D_1, instead of recommended one).

If the MOSFET has a low gate threshold

voltage, $V_{GS(th)}$, then a longer R_2C_1 product will be required than would be the case for a higher $V_{GS(th)}$. This is because the MOSFET with the lower threshold will tend to turn on earlier. If the MOSFET turns on too soon, it will make a low-resistance connection between the supply and the supercapacitor, causing too large a current to flow. A low value of $V_{GS(th)}$ is generally desirable in low-voltage applications, in order to make sure that the MOSFET is turned on as hard as possible after the initial charging phase, to reduce its on-resistance.

The following illustrates how to calculate component values in the circuit in Figure 1. The initial peak current drawn by the current-limiter is determined from Ohm's Law, as follows:

$$\boldsymbol{i_{Peak} = V/R_1} \qquad (1)$$

where V is the supply voltage. Select R_1 according to the initial peak current your application can support.

The next step is to estimate the voltage to which the supercapacitor should be charged (through R_1) before switching on the MOSFET. Assume the maximum current the application can support is i_{MAX}. Since the series resistor, R_1, is still carrying current at the time the MOSFET turns on, this estimate aims for a current of about half the maximum. If the ESR of the supercapacitor is R_S, the on-resistance of the MOSFET is $R_{DS(ON)}$ (at the supply voltage), the voltage on the supercapacitor v_S, the source internal resistance is R_B, and we assume the MOSFET turns on instantly (which is conservative), then the current through the MOSFET at the instant it turns on will be the following:

$$i_{MOSFET} = (V_{Supply} - v_S)/(R_S + R_{DS(ON)} + R_B) = 0.5 i_{MAX} \qquad (2)$$

or, the voltage on the supercapacitor at the moment the MOSFET should turn on is

$$\boldsymbol{v_S = V_{Supply} - 0.5 i_{MAX}(R_S + R_{DS(ON)} + R_B)} \qquad (3)$$

The time (in seconds) at which the supercapacitor reaches this voltage is determined from the following equation:

$$\boldsymbol{t_{ON} = -R_1 C_S \log_e(1 - v_S/V_{Supply})} \qquad (4)$$

t_{ON} is the time after SW_1 has been closed that the MOSFET should switch on. This is the time required for the gate to reach the gate-source threshold voltage, $V_{GS(th)}$, and is given (in seconds) by the following equation:

$$t_{ON} = -R_2 C_1 \bullet \log_e(|V_{GS(th)}| / V_{Supply}) \qquad (5)$$

Re-arranging (5):

$$\boldsymbol{R_2 C_1 = -t_{ON}/\log_e(|V_{GS(th)}| / V_{Supply})} \qquad (6)$$

Choose a value of C_1 such that C_1 >> gate capacitance of the MOSFET, say 1μF, then determine R_2.

The result obtained will be **very** approximate, and the values will need to be adjusted after testing the circuit. It will be necessary to verify that the current does not exceed the desired value, using a few sample MOSFETs in the temperature range of interest. If the current is much lower, then a lower value of R_2 could be tried; if the current is too high, then a larger value of R_2 should be used, to increase the time before the MOSFET is turned on.

When the supply voltage drops to zero (SW_1 is opened and the load discharges the supercapacitor), D_1 discharges C_1 so that the circuit is immediately ready for use again. D_1 need not be a power device, but should at least be able to handle the capacitor's discharge current at the anticipated rate

of fall of the supply voltage. ($i = C_1 dV/dt$, = 1mA for C_1 = 1μF, assuming a very high discharge rate of 1V/ms. Most common small-signal diodes can handle this current.)

Some typical starting values of components are given in Table 1 for a supply source impedance of 150mΩ and supercapacitor ESR of 80 mΩ. Values are as given by the equations, so the designer may wish to choose the next-highest standard resistor value. These values should be modified to obtain the desired behaviour in a real circuit.

Circuit Parameters: Supply voltage V = 4.0V, MOSFET $V_{GS(th)}$ = -1.0V, $R_{DS(ON)}$ = 30mΩ, Source impedance R_B = 150mΩ, and C_1 = 1μF				
i_{MAX} = 400mA				
Supercap Type	**R_1 from (1)**	**v_S from (3)**	**t_{ON} from (4)**	**R_2 from (6)**
GW-02-01 300mF 80mΩ	10	3.95	13.0	9.4MΩ
GW-02-02 380mF 70mΩ	10	3.95	16.7	12MΩ
GW-02-03 450mF 55mΩ	10	3.95	20	14.4MΩ
GW-02-04 800mF 80mΩ	10	3.95	34.7	25MΩ
GW-02-05 220mF 105mΩ	10	3.94	9.35	6.7MΩ
GW-02-06 120mF 60mΩ	10	3.95	5.31	3.8MΩ
i_{MAX} = 1.0A				
GW-02-01 300mF 80mΩ	4	3.87	4.11	3MΩ
GW-02-02 380mF 70mΩ	4	3.88	5.27	3.8MΩ
GW-02-03 450mF 55mΩ	4	3.88	6.35	4.6MΩ
GW-02-04 800mF 80mΩ	4	3.87	11.0	7.9MΩ
GW-02-05 220mF 105mΩ	4	3.86	2.93	2.1MΩ
GW-02-06 120mF 60mΩ	4	3.88	1.68	1.2MΩ

Table 1 Approximate Starting Values of R_1 and R_2 (for a design based on Figure 1) vs Supercapacitor Type and Maximum Supply Current

The value of the capacitance of C_S does not affect the initial peak current. In the design process, C_S would have been chosen to be large enough value to enable the supercapacitor to maintain the supply voltage during load peaks. The ESR of the supercapacitor would also have been selected to optimise the voltage droop during load pulses. The ESR of the CAP-XX device shown in Figure 1 is 80mΩ, which is too small to make a difference to the peak current calculation. Please contact CAP-XX for more information on designing supercapacitors into your application, or visit the CAP-XX web site.

The resistor R_1 dissipates power while the supercapacitor is being charged. In the example shown, a power rating of 0.5W was adequate, even though the power dissipated the instant after SW_1 was closed was 1.6W. The instantaneous power reduced very quickly after switch-on, resulting in only modest heating of R_1. If a higher supply voltage or a larger supercapacitor was used, it might be necessary to increase the resistor's power rating and physical size.

As seen in Figure 4, the total time taken to charge the GW-02-01 supercapacitor to the supply voltage was approximately eight seconds with this circuit configuration, and i_{MAX} = 400mA.

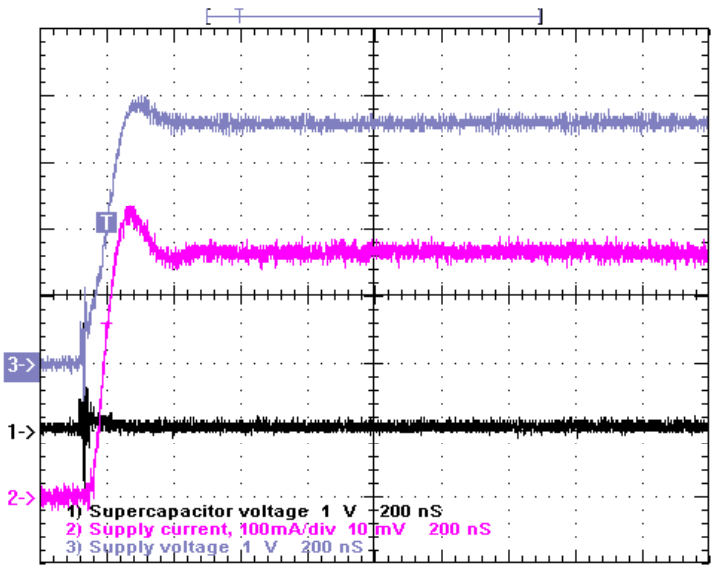

Figure 5 Transient Voltage and Supply Current Response of Circuit in Figure 1

The peak current drawn by the current-limiter circuit when SW_1 is first closed is of interest, as the aim of the circuit is to prevent high currents being drawn from the supply. Figure 5 shows typical current and voltage waveforms for the circuit in Figure 1. The initial current peak is a result of the charging of the MOSFET parasitic capacitances, and the apparently steady current that follows is actually the beginning of the exponential decay curve of the charging of the supercapacitor. The current exceeds the intended limit (400mA) for only a few nanoseconds. This waveform varies somewhat from one switch-on event to the next, depending on how cleanly the switch operates.

MOSFET dv/dt Current-Limiter Design

Refer to Figure 2. The main current-limiting element in this design is the MOSFET, Q_1. This is held in the off state until a short time after SW_1 is closed. This is done by the action of the emitter-follower Q_2, with C_2 initially discharged and providing its base current.

Once enough time has elapsed for C_1 to be fully charged via D_2 and C_S (and/or the load), C_2 has charged via R_4, and Q_2 turns off. This then allows C_1 to begin to discharge via R_3, with a relatively long time constant. When the gate of Q_1 drops to the threshold voltage below Q_1's source voltage (the supply voltage), Q_1 begins to turn on, which starts to charge C_S. Because C_1 is connected to C_S, there is a negative feedback effect: As the voltage on the supercapacitor rises, it tends to turn off Q_1 via C_1.

The rate at which the supercapacitor is charged is thus limited, resulting in an approximately fixed charging current until it is fully charged. Then the MOSFET is finally turned on with the full supply voltage at its gate, resulting in the minimum drain-source resistance that it is possible to get with the given supply voltage. The charging current is determined mainly by the values of C_S, R_3 and C_1, with the characteristics of the MOSFET having a secondary effect. D_3 should have a low reverse current, so that it does not affect the supercapacitor's charging current; likewise, the emitter cutoff current (I_{BEO})of Q_2 is relatively low (less than 10nA, in this case), which has the same advantage.

Although the circuit is slightly more complex than that in Figure 1, it is easier to predict the charging current for particular component values. The current through R_3 during the charging phase is determined from the voltage drop across it, which is just the supply voltage less the threshold voltage of the MOSFET, as follows:

$$i_{R3} = (V_{Supply} - |V_{GS(th)}|)/R_3 \qquad (7)$$

where the positive value, $|V_{GS(th)}|$, is used for convenience.

The rate of change of voltage on C_1 is determined from the current passing through it, as follows, in volts per second:

$$dv_{C1}/dt = i_{R3}/C_1 \qquad (8)$$

Since C_1 is connected to the supercapacitor on the right and its voltage at the gate of the MOSFET tends to remain at the MOSFET's threshold voltage below the supply, the supercapacitor's rate of change of voltage is approximately the same as that of C_1. Therefore, the charging current into the supercapacitor, which is essentially the same as the supply current, is given by the following:

$$i_{Charging} = i_{Supply} = C_S(dv_{C1}/dt) \qquad (9)$$

Combining equations 7, 8 and 9 above, we have:

$$R_3C_1 = Cs \bullet (V_{Supply} - |V_{GS(th)}|) / i_{Charging} \qquad (10)$$

Example: We wish to limit the charging current to 0.4A while using the component values in Figure 2. Hence, if $V_{GS(th)}$ = -1:

$$R_3C_1 = 0.3F \bullet (4.0V - |-1.0V|) / 0.4A = 0.3 \bullet 3 / 0.4\ s = 2.25\ s$$

If we choose C_1 = 220nF, then R_3 = 2.25 / 220x10^{-9} Ω = 10.227MΩ ≈ 10 MΩ

Checking the result with the values chosen, $i_{Charging} = Cs \bullet (V_{Supply} - |V_{GS(th)}|) / R_3C_1$

or $i_{Charging} = 0.3 \bullet 3 / 2.20 = 0.41A$

For a capacitor, $i = C\ dv/dt$. For constant current, this reduces to $i = C\Delta v/\Delta t$, where Δv is the change in voltage across the capacitor in time Δt. Therefore, to charge a supercapacitor from 0V to the supply voltage, the time taken will be:

$$\Delta t = V_{Supply} \bullet C_S / i_{Charging} \qquad (11)$$

In the example above, the time required to charge the supercapacitor is 4.0V•0.3F / 0.41A = 2.93s, which corresponds well with the waveforms in Fig 5.

As in the previous circuit, it is desirable to choose a value of C_1 that is much larger than the input capacitance of the MOSFET, in order to eliminate variability in the charging current and also so that it can be calculated with reasonable accuracy.

D_1 is needed only as a belt-and-braces mechanism to prevent the bipolar transistor, Q_2, from possibly being exposed to reverse base-emitter voltage in those applications where the supply voltage is higher than its limit. (In any event, the current would be limited by R_4.)

D_2 is used to charge C_1 initially, in preparation for its discharge (and re-charging with opposite polarity) via R_3. The value of R_2 is not important, provided it is very much less than that of R_3; a value of 1kΩ could be used instead, for example.

It is necessary that the MOSFET is off initially, so the gate voltage must be kept high enough at first. Subsequently, there is a "dead time" in the circuit, during which the gate voltage is dropping towards its threshold point. The value of the voltage at the junction of C_1 and R_2 just after SW_1 is closed (and C_1 is charged up) effectively determines how long the dead time will be after Q_2 turns off. If the threshold voltage of the MOSFET is very far below this value, it will take some time for the MOSFET to begin to turn on and for charging of the supercapacitor to begin. If this time is too long, a MOSFET with a smaller threshold voltage can be substituted, or the initial gate voltage can be reduced by using two schottky diodes in series at D_2, or by using a silicon diode, such as a 1N914, or equivalent, or by using a series combination of these.

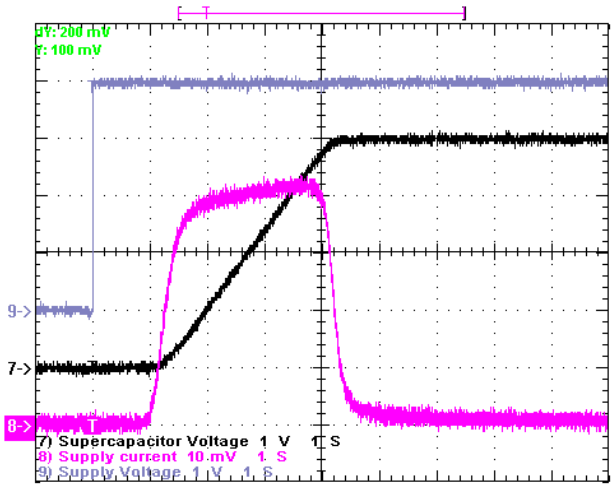

Figure 6 Charging Waveforms Obtained with Circuit in Figure 2, with C_1 = 220nF (using diode with relatively high reverse current as D_3, instead of recommended one).

Diodes D_3 and D_4 discharge the timing capacitors after power-down, so that the circuit is ready to operate again.

The time constant R_4C_2 is not a critical value. It need be long enough only to be sure that C_1 has been charged fully before Q_2 turns off. Bear in mind that there must be sufficient base current available to keep Q_2 on for a short time, while charging C_1.

The following outlines a rough method for choosing Q_2 and estimating required values of R_4 and C_2, for a value of C_1 (determined above). First, note that Q_2 performs two functions: One is to ensure that Q_1 is kept turned off immediately after SW_1 is closed, and the other is to charge C_1 very quickly. Its base drive is provided by C_2, which must therefore be large enough to deliver the drive for long enough to make sure that C_1 is charged. As soon as C_1 is charged, the current-limiting phase of the circuit described above can begin.

Taking advantage of the gain of Q_2, a relatively small capacitance at C_2 enables Q_2 to perform both the above tasks. Q_2 should be a reasonably fast switching transistor with reasonably high gain. The minimum gain of a 2N2222A (or 2N2222) varies quite widely (for example, 35 to 100 at V_{CE} = 10V), but it should be adequate. There are, no doubt, many equivalent or better devices, both surface-mounting and through-hole types.

By design, C_1 is much larger than the input capacitance of the MOSFET, so the latter is insignificant. Provided Q_2 has the gain of a 2N2222A or better, then a value of C_2 that is comparable to that of C_1 should be adequate. That is, something in the range of 0.5C$_1$ to $2C_1$ (or more, if desired) is expected to work.

Next, we need to determine R_4. This is found from the time constant R_4C_2. C_1 should charge relatively quickly via D_2 when SW_1 closes, but it is difficult to estimate just how long it takes to charge. The value of R_2 chosen in Figure 2 was selected to give what is really quite a large time constant (10ms) relative to the expected time to charge C$_1$, but this is still negligible relative to the time required to charge the supercapacitor, so it has no real detrimental effect. Making R_4 too small (say, sub-1kΩ) may contribute to the transient initial current that flows when SW_1 is closed, which is undesirable. If R_4 is very high (say, in the range >>1MΩ, with a correspondingly low value of C_2), Q_2 may not turn off properly.

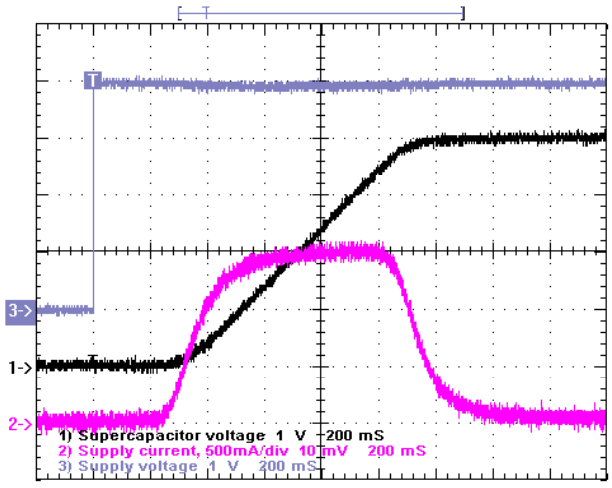

Figure 7 Charging Waveforms Obtained with Circuit in Fig. 2, with C_1 = 56nF (and D_3 with high reverse current).

As seen in figure 6, the current during charging is relatively constant. There is a 1s dead-time in this example, and this could be reduced by the measures described above. Even with the dead time, the total charging time is just over 4s,

compared with approximately 8s for the circuit in figure 1, when using approximately the same peak current.

Figure 7 shows the circuit of Figure 2 with a charging current of approximately 1.5A. The dead time before charging begins is only about 250ms with this value of C_1, and the total time to charge the supercapacitor is about 1.2s.

Table 2 is a list of some component values for different charging currents, using the circuit in Figure 2.

Circuit Parameters: Supply voltage V = 4.0V, and MOSFET $V_{GS(th)}$ = -1.0V						
$i_{Charging}$ = 400mA						
Supercapacitor	R_3C_1 from (10), s	Select C_1, nF	Calc. R_3, Ω	Select R_4C_2, s	Select C_2, nF	Calc. R_4, Ω
GW-02-01 300mF 80mΩ	2.25	220	10M	0.01	470	21.2k
GW-02-02 380mF 70mΩ	2.85	220	13M	0.005	330	15k
GW-02-03 450mF 55mΩ	3.375	330	10.5M	0.01	330	30.1k
GW-02-04 800mF 80mΩ	6	220	27.4M	0.01	220	45.3k
GW-02-05 220mF 105mΩ	1.65	220	7.5M	0.01	220	45.3k
GW-02-06 120mF 60mΩ	0.9	180	4.99M	0.01	220	45.3k
$i_{Charging}$ = 1.0A						
GW-02-01 300mF 80mΩ	0.9	180	4.99M	0.01	150	66.5k
GW-02-02 380mF 70mΩ	1.14	180	6.34	0.01	150	66.5k
GW-02-03 450mF 55mΩ	1.35	180	7.5M	0.01	220	45.3k
GW-02-04 800mF 80mΩ	2.4	180	13.3M	0.01	220	45.3k
GW-02-05 220mF 105mΩ	0.66	330	2M	0.005	220	22.6k
GW-02-06 120mF 60mΩ	0.36	330	1.1M	0.005	220	22.6k

Table 2 Examples of Values of R_3, C_1, R_4 and C_2 for a design based on Figure 2 vs Supercapacitor Type and Maximum Supply Current

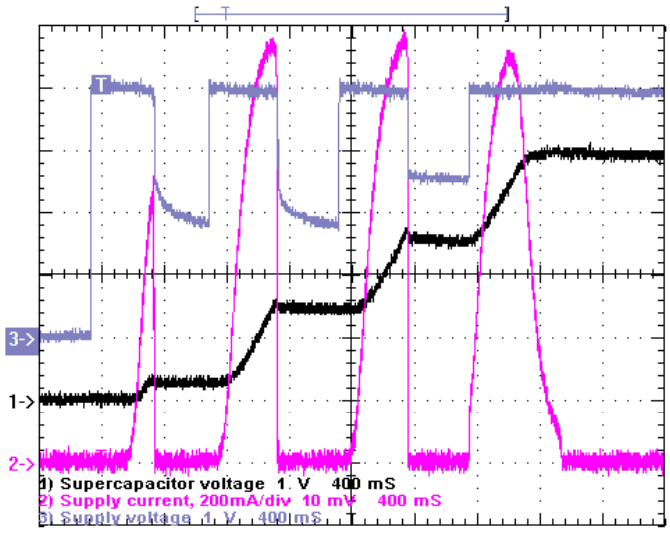

Figure 8 Charging Waveforms Obtained with Circuit in Figure 2, with C_1 = 56nF, and with SW_1 Repeatedly Opened and Closed.

Figure 8 illustrates the robustness of the circuit in Figure 2 when SW_1 is repeatedly opened and closed while charging is in progress. Each time the switch is closed again, the charging continues from where it left off, without the current rising to excessive levels.

Figure 9 shows the transient supply current and the voltage waveforms obtained with the circuit in Figure 2. The current peak on closing the switch results from charging C_1 and from the charging of the parasitic capacitances of the MOSFET. The peak current is about 500mA for several nanoseconds, after which it falls to nearly zero and remains there until charging of the supercapacitor begins.

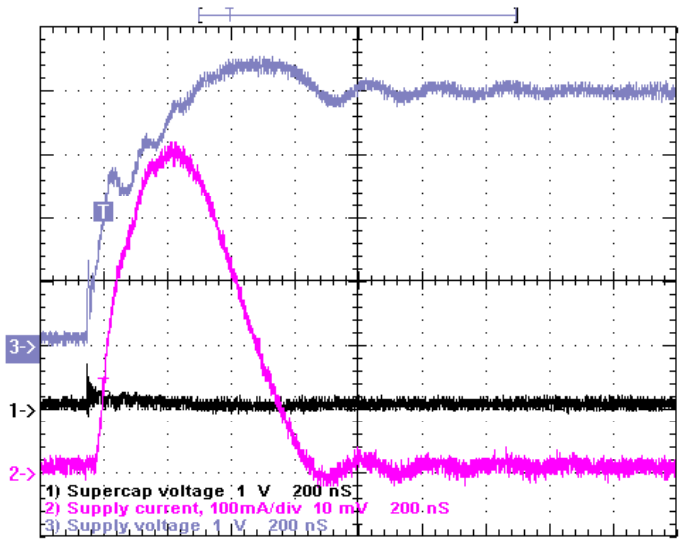

Figure 9 Initial Transient Waveforms Obtained with Circuit in Figure 2, with *C1* = 56nF.

Feedback Control Design

Figure 3(a) is a current-limiter circuit that monitors the actual current and uses feedback to control current flow through the MOSFET. The supercapacitor charged by the circuit is represented by CX1. It has two cells in series, and its associated balancing resistors are R_5 and R_8. The limiting current value is independent of the supercapacitor value and there are therefore no tables of suitable supercapacitors presented here.

The circuit in Figure 3(b) detects when the voltage on the supercapacitor has reached a predetermined value and outputs a "POWER GOOD" (active high) signal that may be used to signal to other circuits that the supercapacitor is fully charged. The circuits (a) and (b) are designed to operate from a nominal 3.3V supply, although they will function at voltages at least as low as 3V and (preferably with suitable resistor changes) up to 4.5V, the rated voltage of the two-cell supercapacitor.

The circuit in (a) monitors the current by comparing the voltage drop across a shunt resistor (R_1) with a reference voltage derived from a low-power voltage reference IC. If the voltage across the shunt exceeds the reference value, the current is too high and the operational amplifier output begins to turn off the MOSFET, M_1. When the supercapacitor is charged, the current drops and M_1 is turned on fully again.

If the optional "ENABLE" circuit is included, then a logic 0 signal (0V) applied to the input is required to enable the current-limiter circuit to operate; if the input is high or left floating, then M_1 is held off by M_2, with the result that there is no current flow to the load.

The voltage reference circuits D_1, D_5 and D_7 were selected for their accuracy and low power consumption. It may be possible to replace these with cheaper zener diodes, if required, provided the parts used have good tolerances (preferably 1%) across the temperature range of operation, otherwise the limit current and the voltage at which the POWER GOOD signal is generated might be incorrect. Zener diodes will typically require higher bias currents, resulting in increased power consumption by the circuit.

The operational amplifier TS1852A has a maximum input offset voltage of 1mV and a typical value of 0.1mV. Since this parameter affects the accuracy of the limit current and the POWER GOOD

signal, amplifiers with higher offset voltages should not be used. Note also that if the POWER GOOD circuit is used separately, its operational amplifier's power supply should be bypassed with a 100nF capacitor.

The POWER GOOD circuit in (b) compares a proportion of the voltage across the supercapacitor with a reference voltage. When the supercapacitor's voltage exceeds a predetermined value, the POWER GOOD output goes high. Some hysteresis is introduced via the feedback resistor, R_{22}.

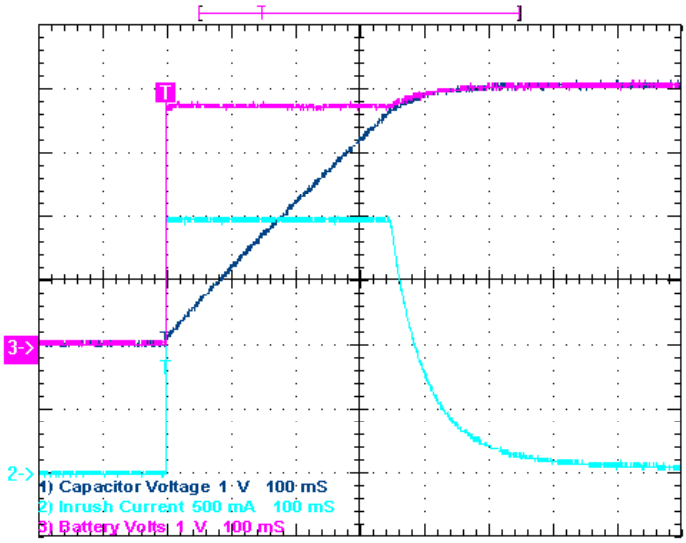

Figure 10 Voltage and Current Waveforms from Circuit in Figure 3. Component Values Selected for Battery Voltage 4.2V, Current Limit 2A.

Figure 10 shows the voltage and current waveforms for a circuit of the type in Figure 3, with components selected for a 2A current limit. The Lithium-ion battery supplying the circuit had a fully-charged voltage of 4.2V. During the current-limiting period in Figure 10, the battery voltage was reduced by the voltage drop in its internal resistance under load.

Relationship between maximum current and component values: The current limit in Figure 3(a) may be selected by appropriate choice of the resistors in the voltage divider across the reference voltage, i.e., R_2 and R_6. First, the shunt voltage when the current is at its limiting value is given by

$$v_{R1} = i_{Lim} \cdot R_1 \qquad (12)$$

The voltage at the non-inverting input of the operational amplifier at the moment the current-limiting begins will be

$$v_+ = \frac{R_2}{R_2 + R_6} V_{D1} \qquad (13)$$

where V_{D1} is the voltage across D_1. Equating (12) and (13), we have the following result for the limiting current as a function of the resistor values:

$$i_{Lim} = \frac{R_2}{R_1 (R_2 + R_6)} V_{D1} \qquad (14)$$

Alternatively, we may express the value of R_2 in terms of the desired maximum current and the other values, as follows:

$$R_2 = \frac{i_{Lim} R_1 R_6}{V_{D1} - i_{Lim} R_1} \qquad (15)$$

Example: Using the values given in Figure 3, which include a 1.2V reference for D_1, and if the desired maximum current is 500mA, Equation 15 gives 203Ω for the value of R_2.

Relationship between POWER GOOD threshold voltage on the supercapacitor and the component values: Refer to Figure 3(b). If the output of the operational amplifier is low because the voltage on the supercapacitor is low, then the voltage at the non-inverting input may be shown to be the following:

$$v_{+(PGLow)} = \frac{v_{S(PGLow)}}{R_{17}(1/R_{20} + 1/R_{22}) + 1} \qquad (16)$$

where $v_{S(PGLow)}$ is the voltage on the supercapacitor. Likewise, if the output of the operational amplifier is high because the voltage on the supercapacitor is above the reference value, then the voltage at the non-inverting input may be shown to be the following:

$$v_{+(PGHigh)} = \frac{v_{S(PGHigh)}R_{20}R_{22} + V_{D7}R_{17}R_{20}}{R_{17}R_{22} + R_{20}R_{22} + R_{17}R_{20}} \qquad (17)$$

where V_{D7} is the voltage on the reference device connected to R_{22}. However, the switching points in the POWER GOOD signal occur when each of $v_{+(PGLow)}$ and $v_{+(PGHigh)}$ is equal to the voltage at the inverting input. The reference voltage at the inverting input to the amplifier is given by the following:

$$v_{-} = \frac{R_{16}}{R_{14} + R_{16}} V_{D5} \qquad (19)$$

where V_{D5} is the voltage at the reference IC/diode, D_5. The supercapacitor voltage at which the POWER GOOD signal changes from low to high as the supercapacitor charges is when $v_{+(PGLow)}$ (Equation 16) is equal to v_{-} (Equation 19), as follows:

$$v_{s(PGLow)} = \frac{V_{D5}R_{16}[R_{17}(1/R_{20} + 1/R_{22}) + 1]}{R_{14} + R_{16}} \qquad (20)$$

Similarly, the supercapacitor voltage at which the POWER GOOD signal changes from high to low as the supercapacitor discharges is found by equating $v_{+(PGHigh)}$ (Equation 17) and v_{-} (Equation 19), as follows:

$$v_{s(PGHigh)} = \frac{V_{D5}R_{16}(R_{17}R_{22} + R_{20}R_{22} + R_{17}R_{20})}{R_{20}R_{22}(R_{14} + R_{16})} - V_{D7}\frac{R_{17}}{R_{22}} \qquad (21)$$

NOTE: As discussed above, "PGLow" and "PGHigh" refer to the state of the POWER GOOD signal at the time the voltage on the supercapacitor is considered. The effect of hysteresis is that the voltage $v_{S(PGLow)}$ is higher than the voltage $v_{S(PGHigh)}$.

Example: Using the component values given in Figure 3, which include 2.5V reference devices as D_5 and D_7, the POWER GOOD circuit has a nominal switching voltage of 3.0V (from Equation 19). When the supercapacitor is charging, the voltage at which POWER GOOD goes from low to high is $v_{S(PGLow)}$= 3.07V (from Equation 20). When the supercapacitor is discharging, the voltage at which POWER GOOD goes from high to low is $v_{S(PGHigh)}$= 2.93V (from Equation 21).

Figure 11 shows the transient behaviour of the circuit in Figure 3, using components that give a current limit of 2A, as in Figure 10. The circuit was disconnected from the battery and allowed to discharge the supercapacitor to about 3V. It was then re-connected to the battery, resulting in a current of about 3.5A for 80μs before the current-limiter responded, limiting the subsequent current to 2A. The upper waveform at the right was the battery voltage during the current-limiting phase; the supercapacitor's voltage rose subsequent to re-connection to the battery, but the slope is not discernable in the short time covered by this trace.

A host device with sufficient decoupling on its supply could deliver the transient 3.5A current without resetting itself.

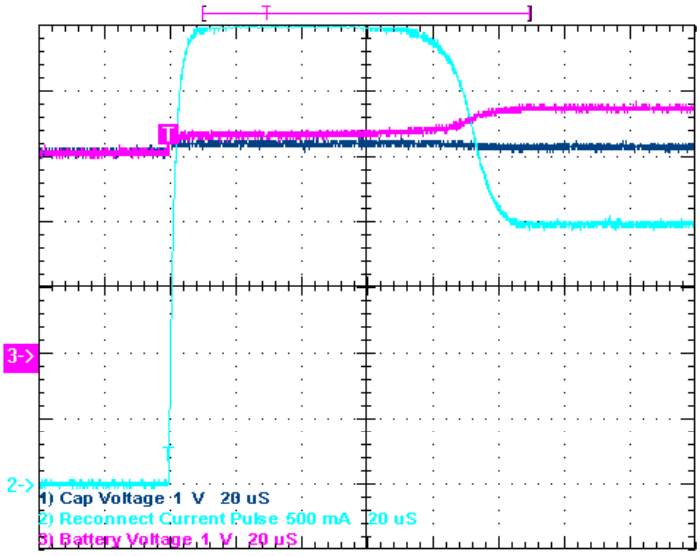

Figure 11 Transient Response of Circuit in Figure 3, with Components Selected for Current Limit of 2A, Showing Re-Connection of the Circuit to the Battery Following Partial Discharge of Supercapacitor.

Further Information

CAP-XX will be pleased to provide further information on the applications described here, and on the use of supercapacitors in any application. Please use the contact details at the foot of the page, or visit the CAP-XX web site.

This Application Note is available on the CAP-XX web site. On the same web page may be found a downloadable copy of a spreadsheet containing the equations used to calculate the component values, above.

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