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HW101 / HW201 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HW101 is a single cell supercapacitor. The HW201 is a dual cell supercapacitor with two HW101 cells in series, so HW201 capacitance = Capacitance of HW101/2 and HW201 ESR = 2 x HW101 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HW101		0		2.9	V
		HW201				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HW101		0		2.75	V
		HW201		0		5.5	
Capacitance	C	HW101	DC, 23°C	608	760	912	mF
		HW201		304	380	456	
ESR	ESR	HW101	DC, 23°C		50	60	mΩ
		HW201			100	120	
Leakage Current	I_L		2.75V, 23°C 120hrs		1	2	µA
RMS Current	I_{RMS}		23°C			3	A
Peak Current[1]	I_P		23°C			30	A

[1]Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HW101F	**1.3mm**	No adhesive tape on underside of the supercapacitor	**HW101G**	**1.4mm**	Adhesive tape on underside, release tape removed
HW201F	**2.7mm**		**HW201G**	**2.8mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

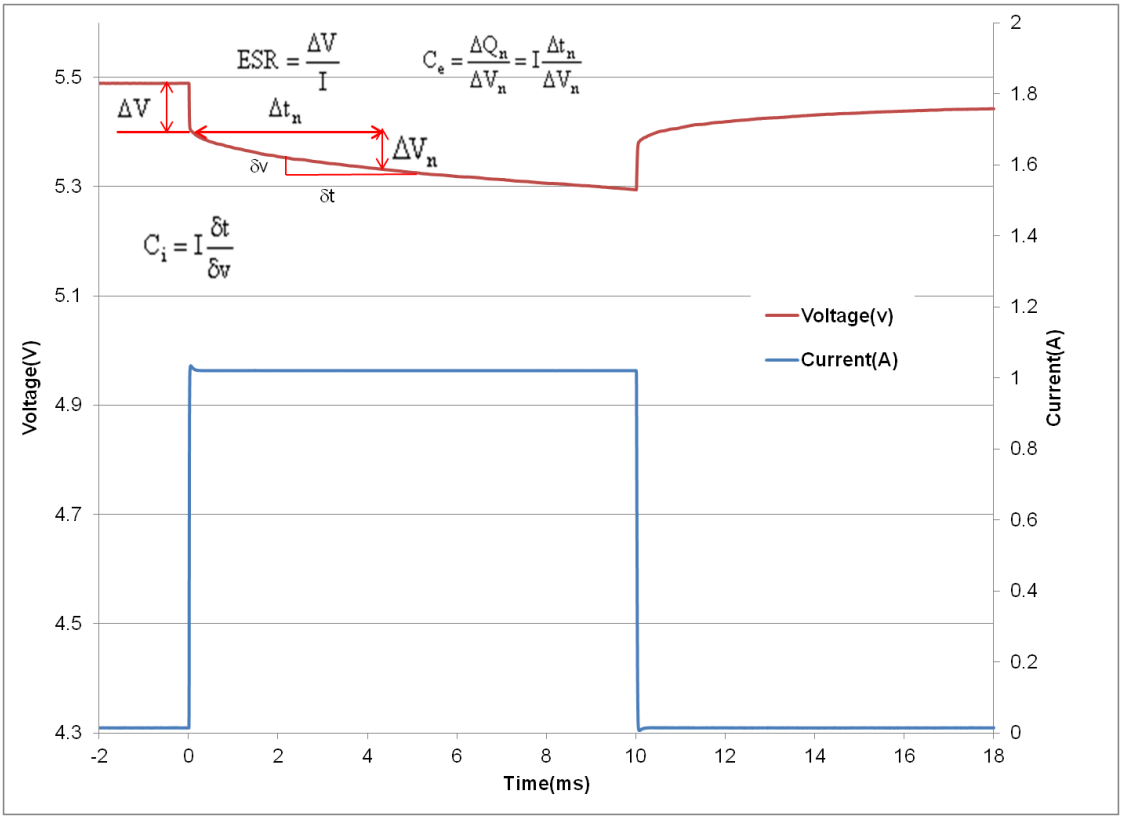

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HW201

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.489V-5.413V)/1A = 76mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I \times \Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.413 V – 5.354V) = 59mV. Therefore Ce(2ms) = 1A x 2ms/59mV = 33.9mF. After 10ms, the voltage drop = 5.413 V – 5.295V = 118mV. Therefore Ce(10ms) = 1 A x 10ms/118mV = 84.7mF. The DC capacitance of an HW201 = 0.38 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

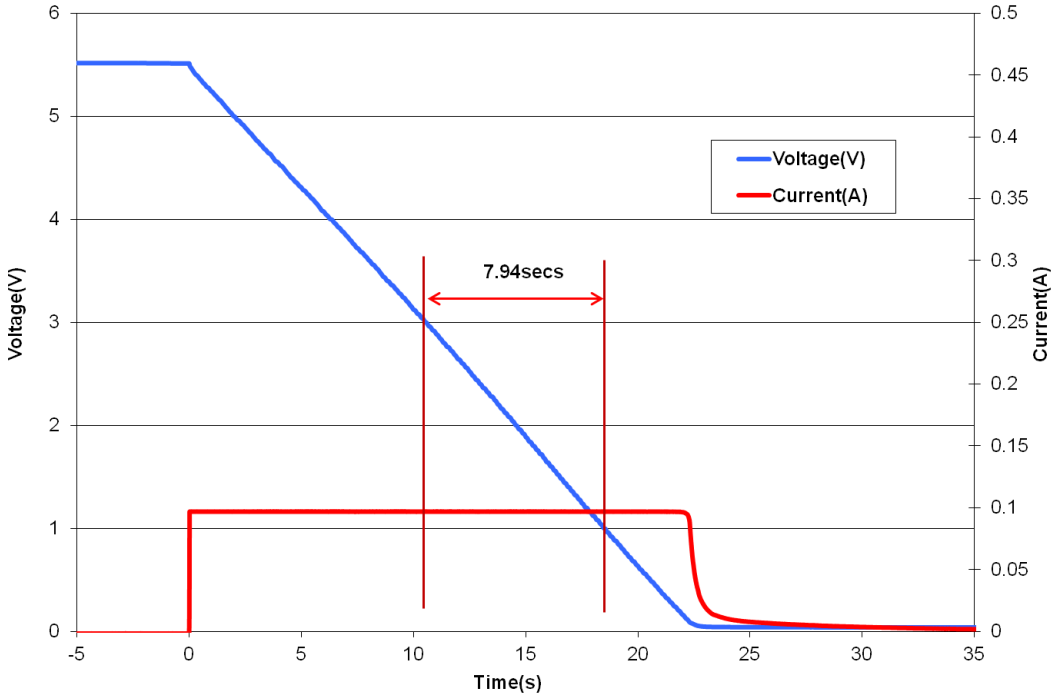

Fig 2: Measurement of DC Capacitance for an HW201

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 7.94s /2V = 397mF, which is well within the 380mF +/- 20% tolerance for an HW201 cell.

Measurement of ESR

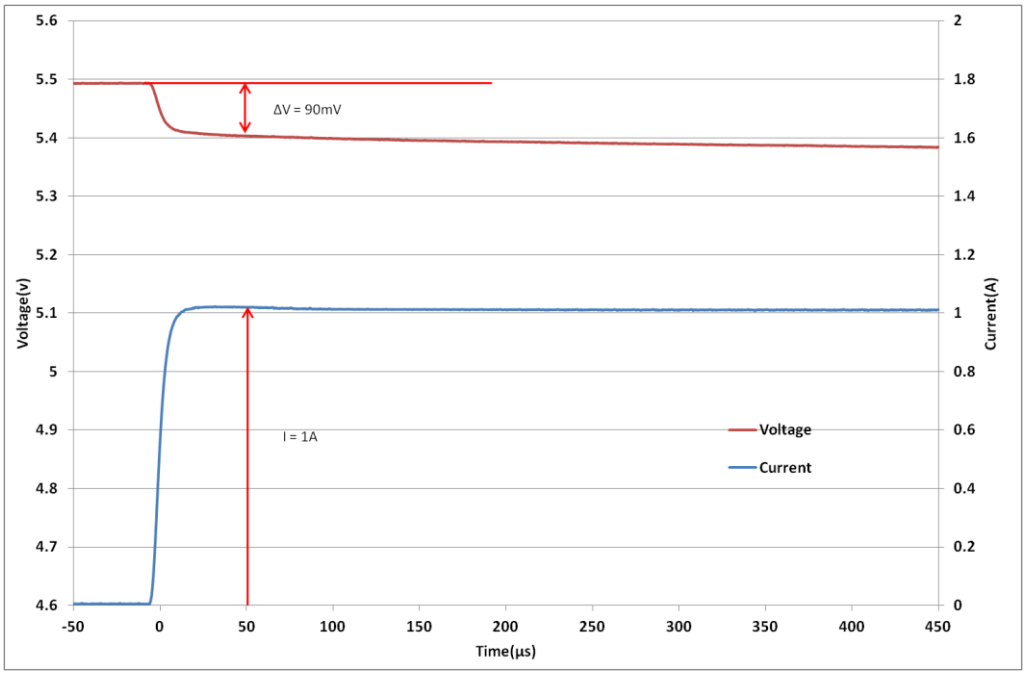

Fig 3: Measurement of ESR for an HW201

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 90mV/1A = 90mΩ.

Effective Capacitance

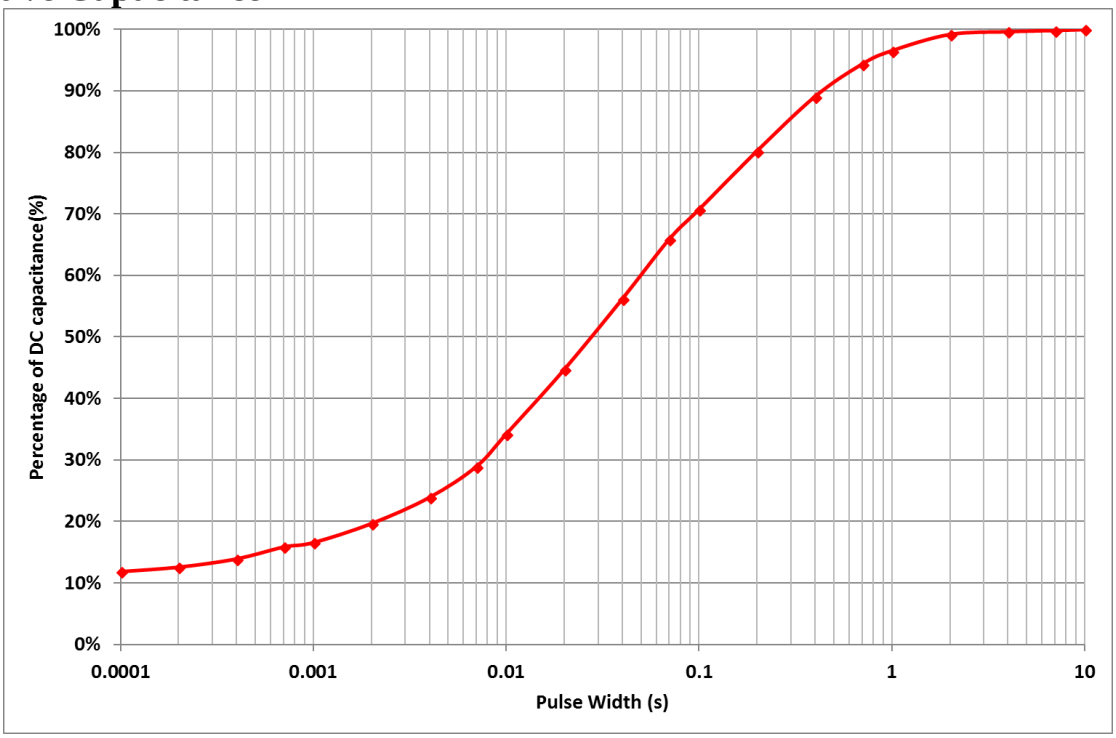

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HW101, HW201 @ 23°C. This shows that for a 1ms PW, you will measure 17% of DC capacitance or 129mF for an HW101 or 65mF for an HW201. At 10ms you will measure 34% of the DC capacitance, and at 100ms you will measure 71% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10ms, then you would use the Ceff(10ms) = 34% of DC capacitance = 129mF for an HW201, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 100mΩ + 1A x 10ms / 129mF = 178mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

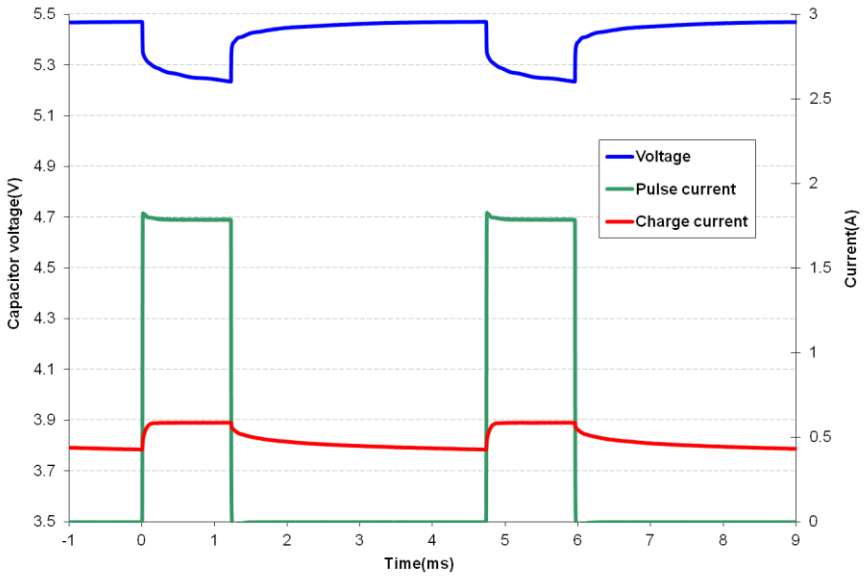

Fig 5 shows that the HW201 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 34.2mF coupled with the low ESR supports this pulse train with only ~230mV droop in the supply rail.

Fig 5: HW201 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

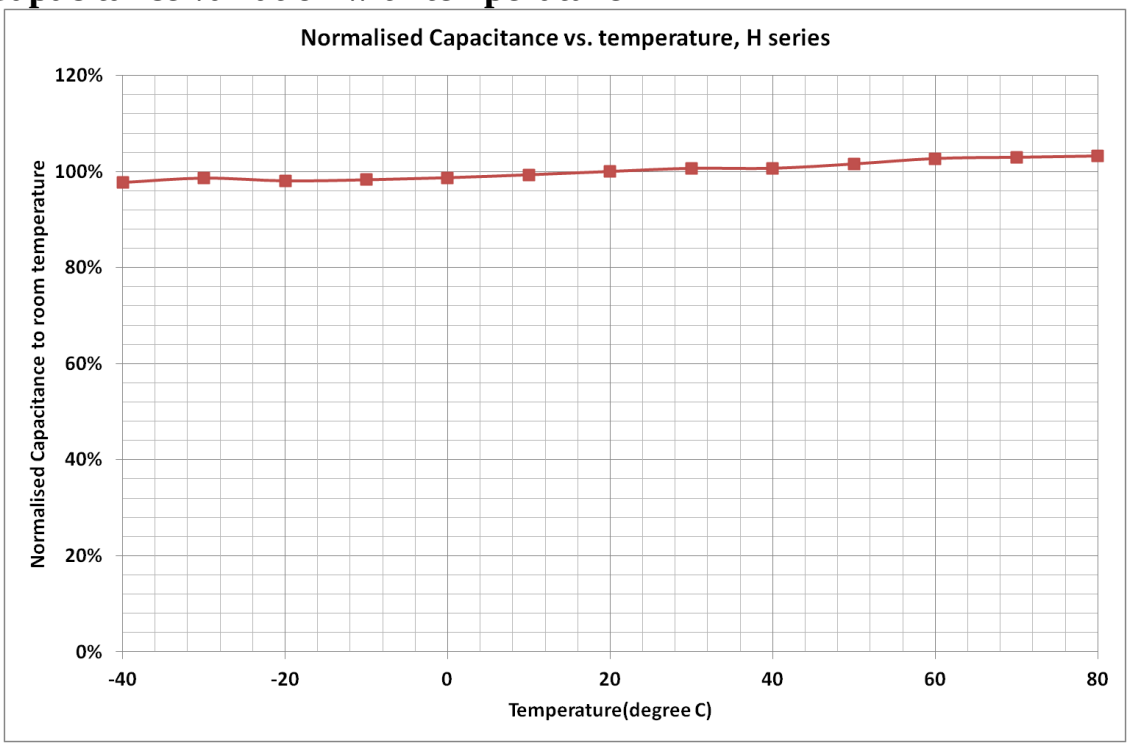

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

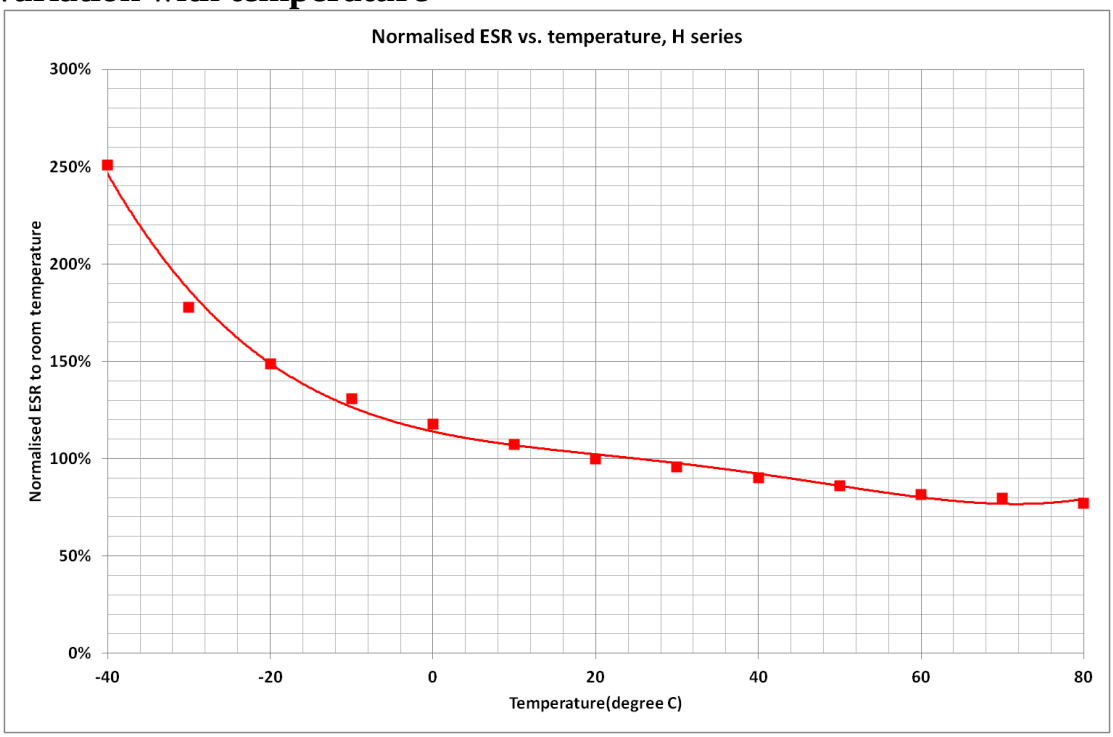

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.5 x ESR at room temp, and that ESR at 70°C is ~0.8 x ESR at room temperature.

Frequency Response

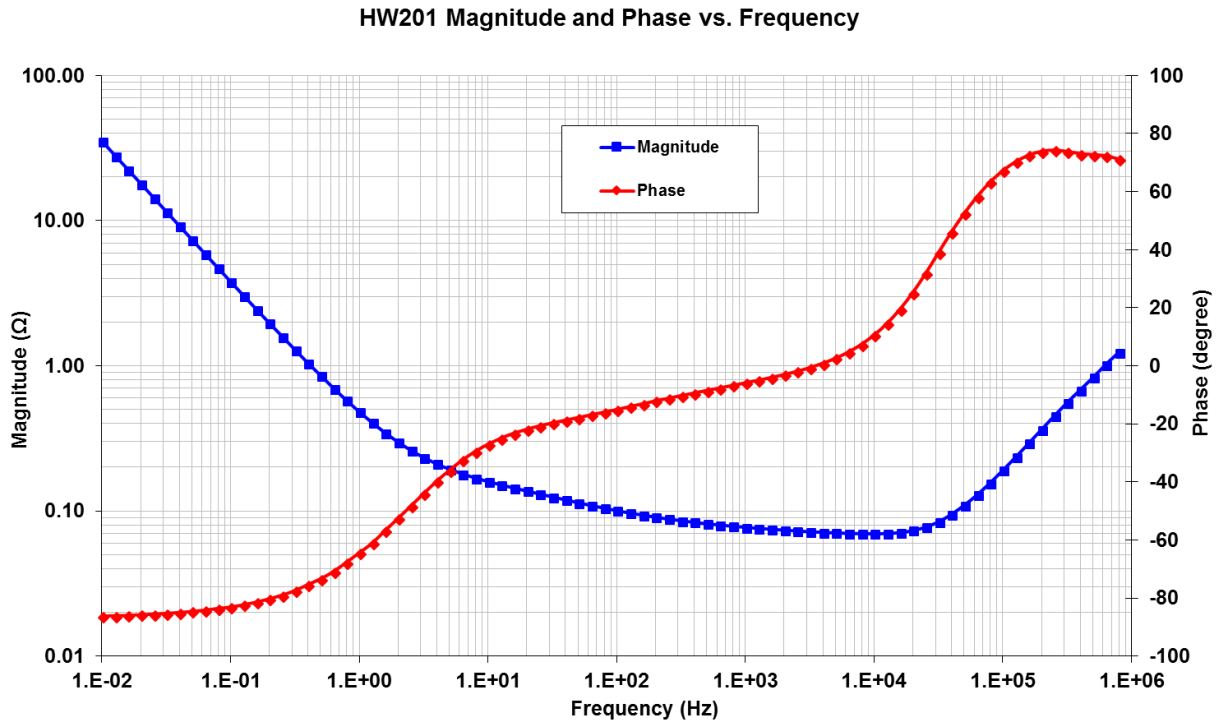

Fig 8: Frequency Response of Impedance (biased at 5.5V with a 50mV test signal)

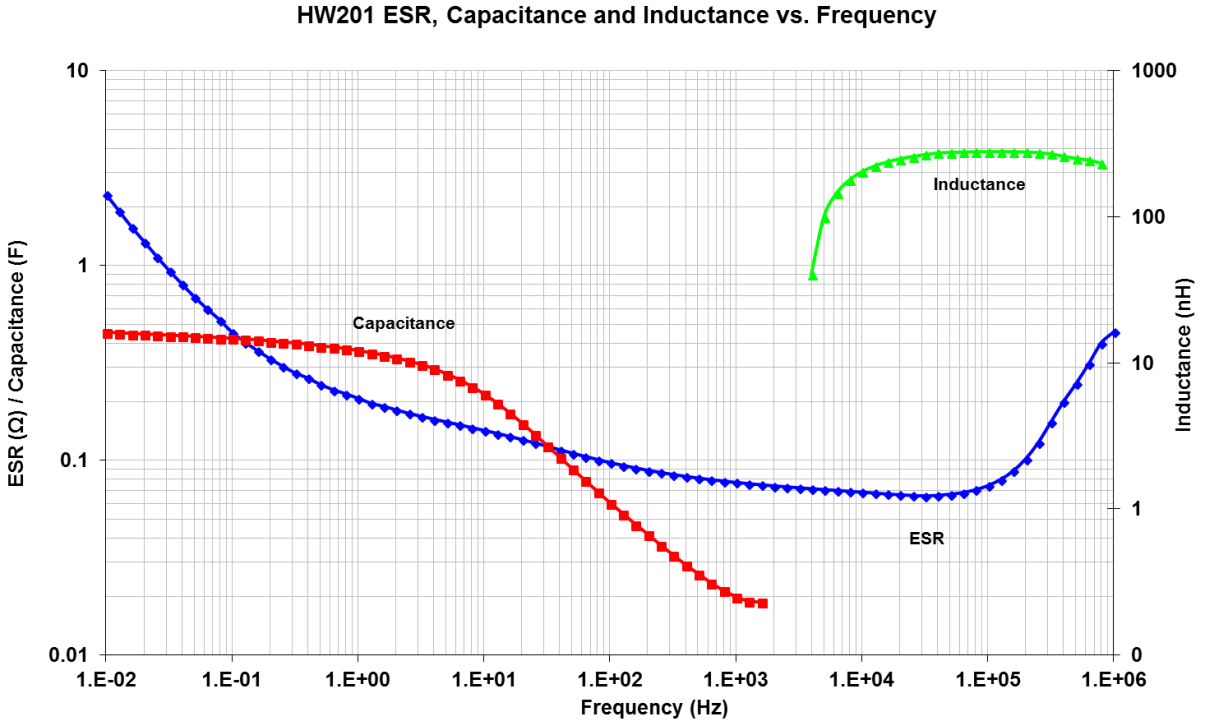

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 3 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

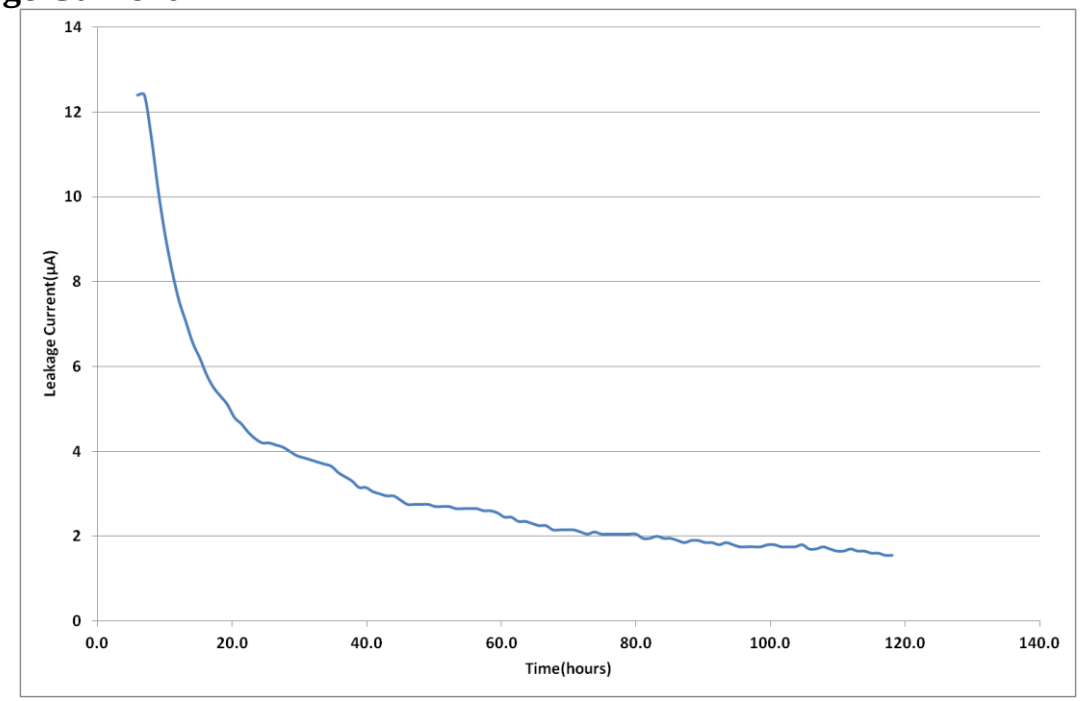

Fig 10: Leakage Current

Fig 10 shows the leakage current for HW101 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1.5µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

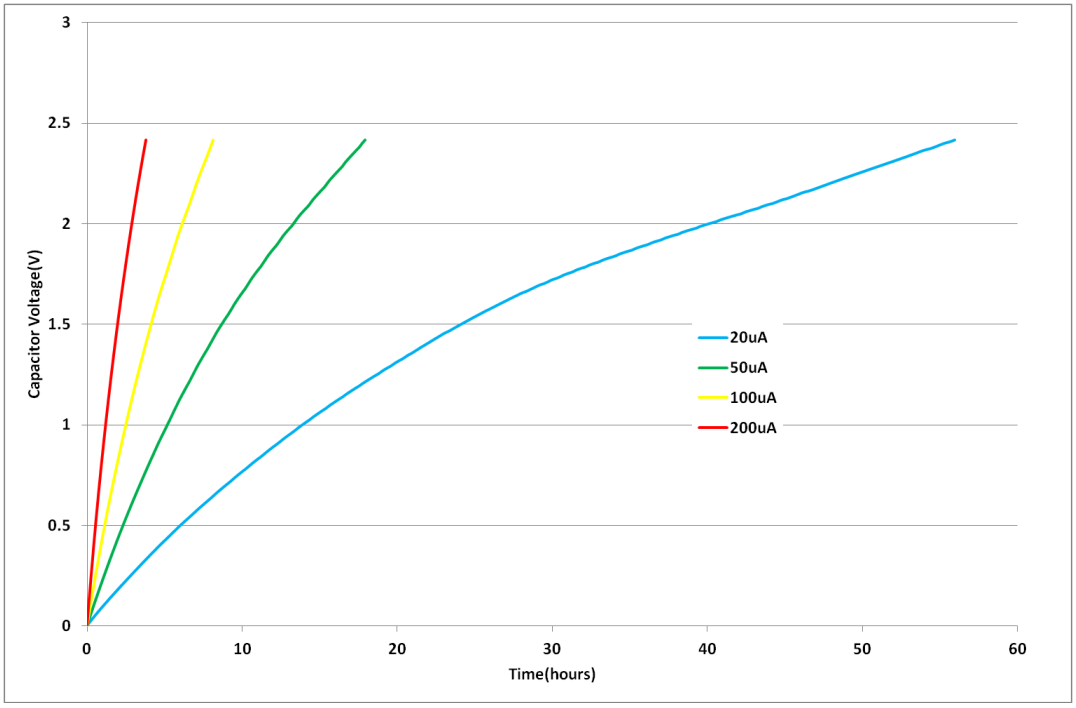

Fig 11: Charging an HW101 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 0.76F x 2.4V / 0.00002A = 25hrs to charge a 0.76 F supercapacitor to 2.4V at 20µA, but Fig 11 shows it took 56hrs. At 100µA charging occurs at a rate close to the theoretical rate.

RMS Current

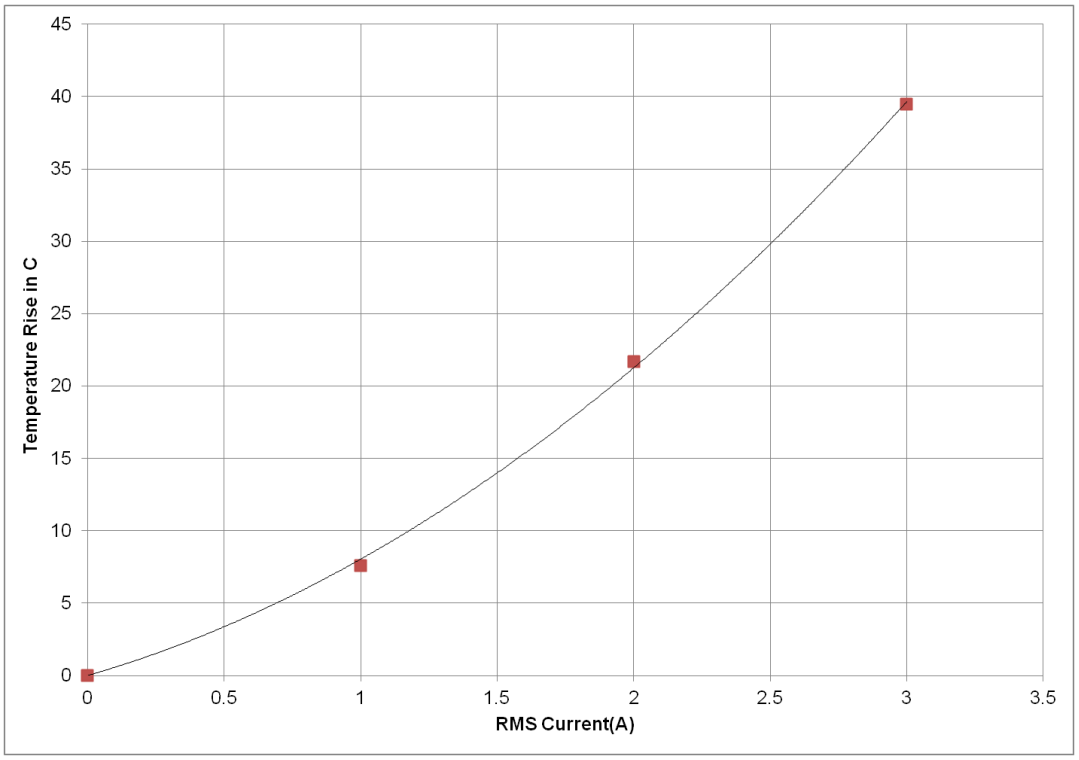

Fig 12: Temperature rise in HW201 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 2.5A, which causes a 30°C temperature increase.

CAP-XX Supercapacitors Product Guide

Refer to the package drawings in the CAP-XX Supercapacitors Product Guide for detailed information of the product's dimensions, PCB landing placements, active areas and electrical connections.

Refer to the CAP-XX Supercapacitors Product Guide for information on endurance and shelf life, transportation and storage, assembly and soldering, safety and RoHS/EREACH certification.

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HW102 / HW202 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HW102 is a single cell supercapacitor. The HW202 is a dual cell supercapacitor with two HW102 cells in series, so HW202 capacitance = Capacitance of HW102/2 and HW202 ESR = 2 x HW102 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HW102		0		2.9	V
		HW202				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HW102		0		2.75	V
		HW202		0		5.5	
Capacitance	C	HW102	DC, 23°C	320	400	480	mF
		HW202		160	200	240	
ESR	ESR	HW102	DC, 23°C		40	48	mΩ
		HW202			75	84	
Leakage Current	I_L		2.75V, 23°C 120hrs		1	2	µA
RMS Current	I_{RMS}		23°C			6	A
Peak Current[1]	I_P		23°C			30	A

[1]Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HW102F	**1.3mm**	No adhesive tape on underside of the supercapacitor	**HW102G**	**1.4mm**	Adhesive tape on underside, release tape removed
HW202F	**2.7mm**		**HW202G**	**2.8mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

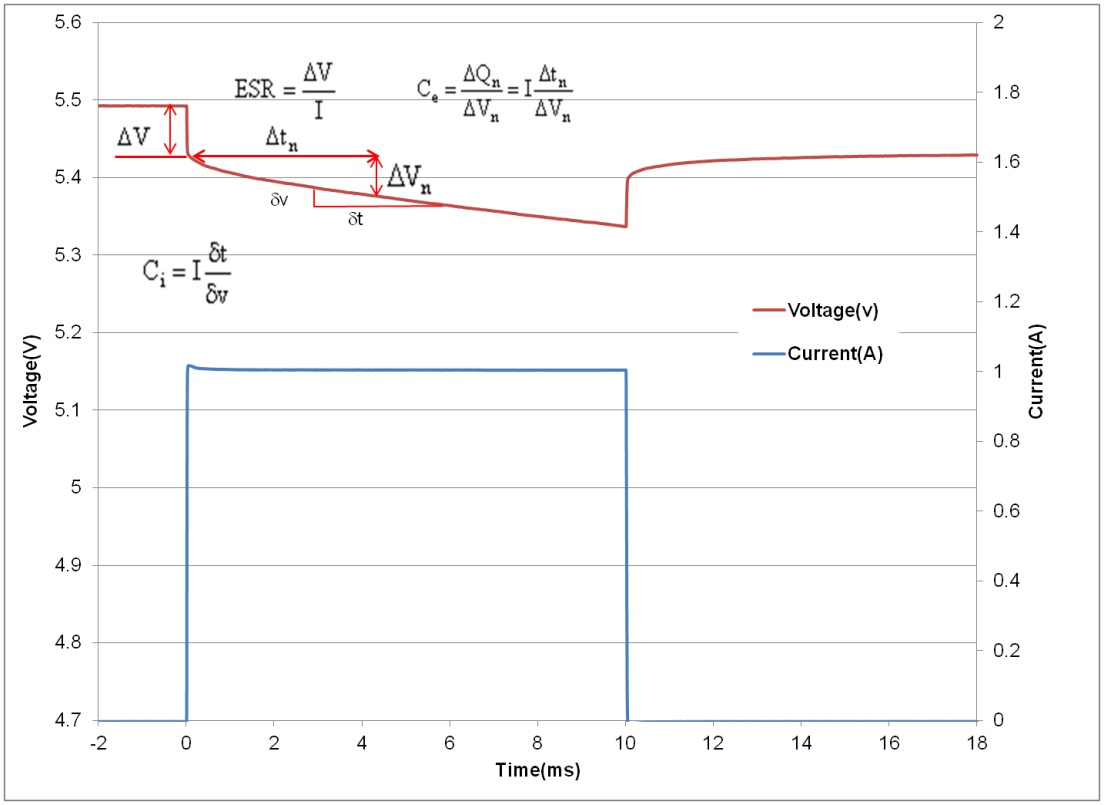

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HW202

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.492V-5.438V)/1A = 54mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I \times \Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.438 V – 5.394V) = 44mV. Therefore Ce(2ms) = 1A x 2ms/44mV = 45.5mF. After 10ms, the voltage drop = 5.438 V – 5.337V = 101mV. Therefore Ce(10ms) = 1 A x 10ms/101mV = 99mF. The DC capacitance of an HW202 = 0.2 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

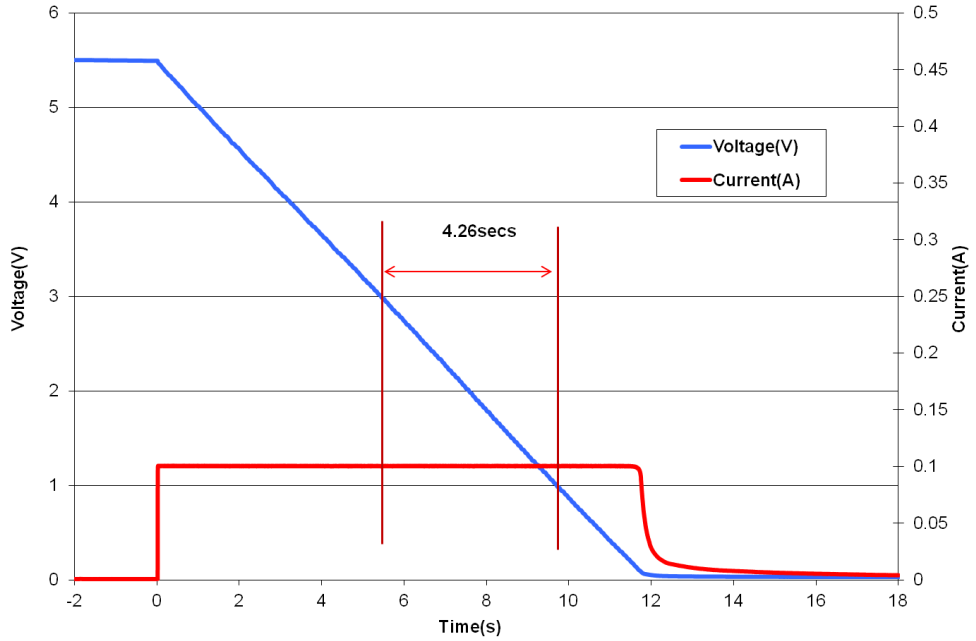

Fig 2: Measurement of DC Capacitance for an HW202

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 4.26s /2V = 213mF, which is well within the 200mF +/- 20% tolerance for an HW202 cell.

Measurement of ESR

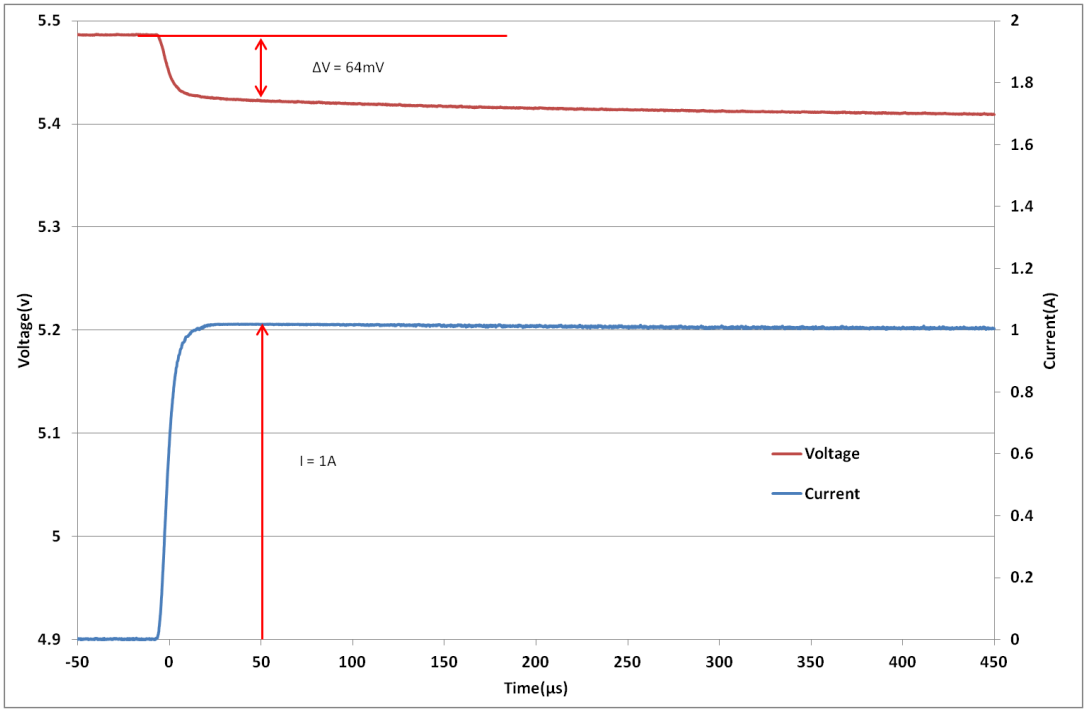

Fig 3: Measurement of ESR for an HW202

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 64mV/1A = 64mΩ.

Effective Capacitance

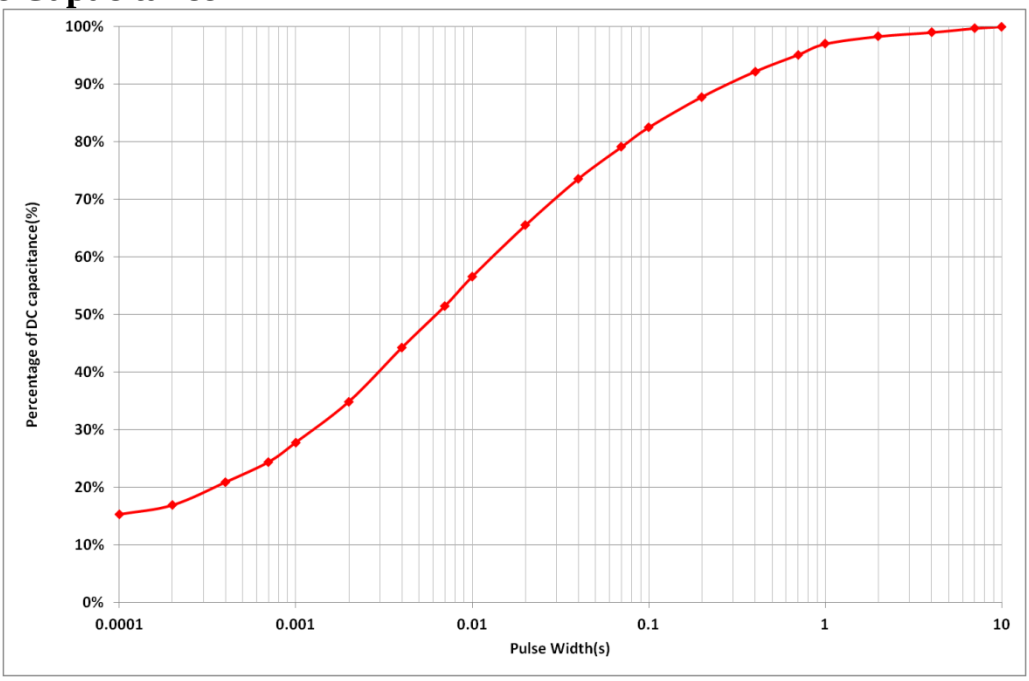

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HW102, HW202 @ 23°C. This shows that for a 1msec PW, you will measure 28% of DC capacitance or 112mF for an HW102 or 56mF for an HW202. At 10msecs you will measure 57% of the DC capacitance, and at 100msecs you will measure 83% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10msecs, then you would use the Ceff(10msecs) = 57% of DC capacitance = 114mF for an HW202, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 65mΩ + 1A x 10ms / 114mF = 152.7mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

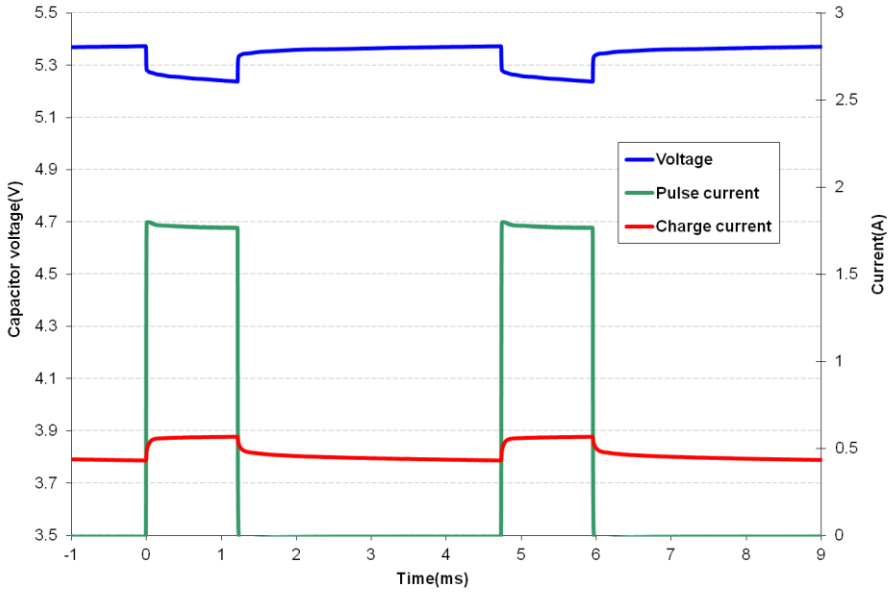

Fig 5 shows that the HW202 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 56mF coupled with the low ESR supports this pulse train with only ~133mV droop in the supply rail.

Fig 5: HW202 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

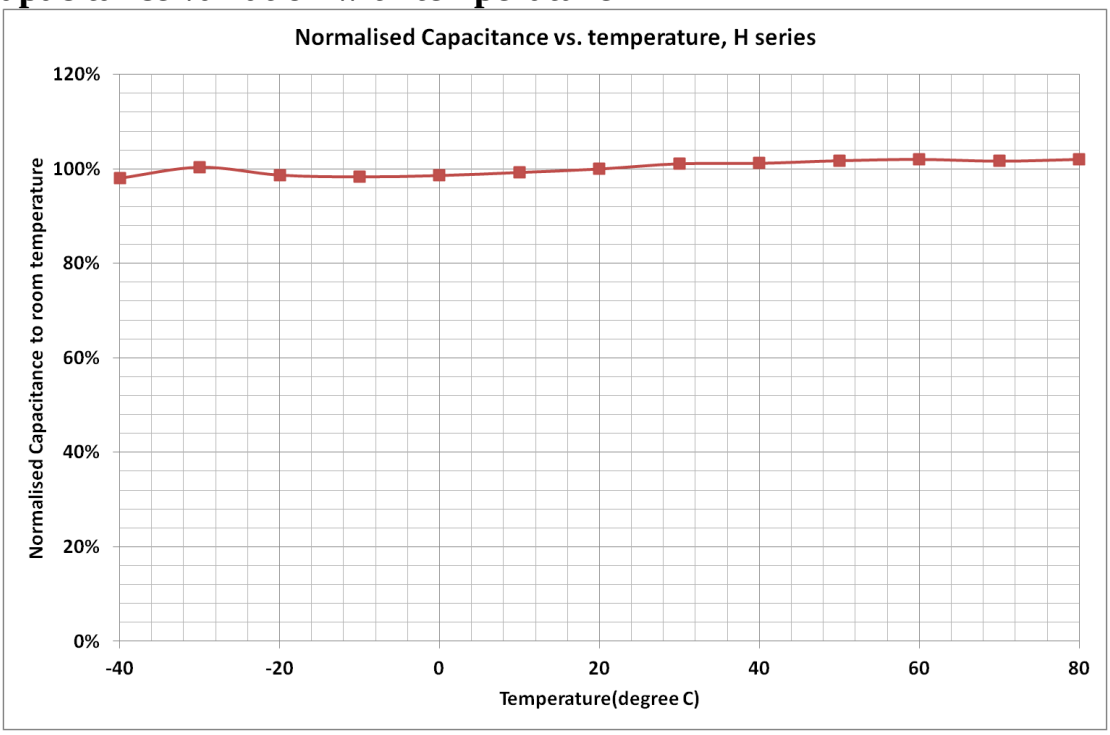

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

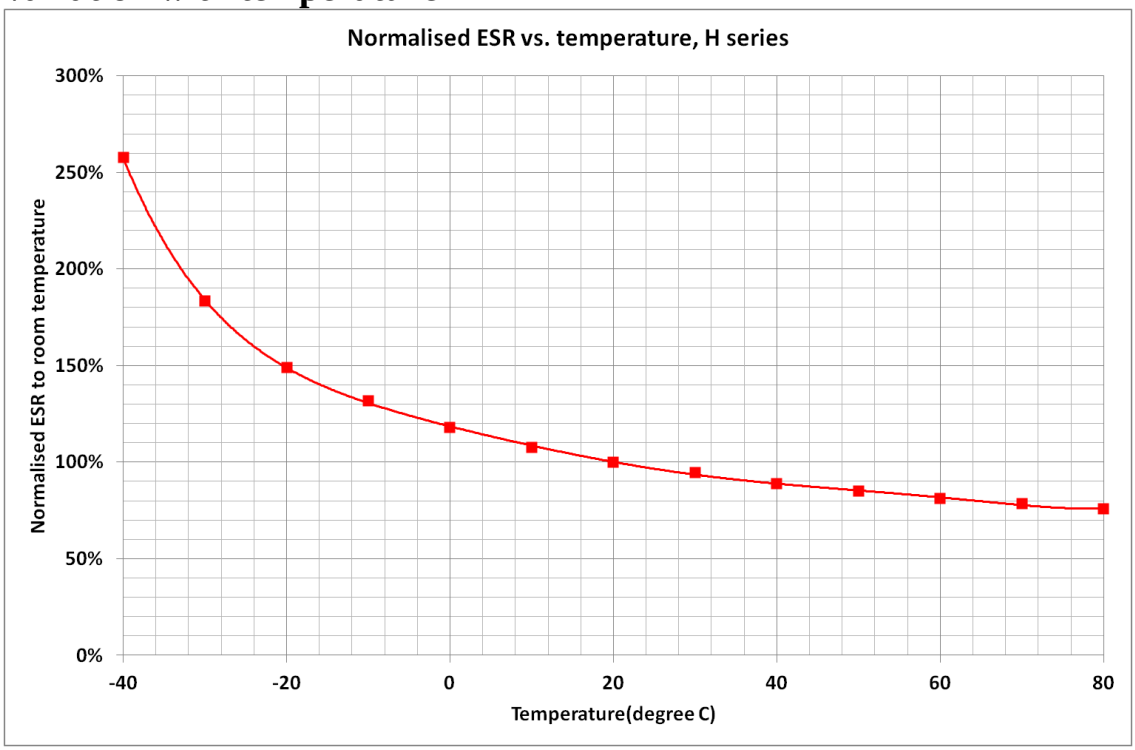

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.6 x ESR at room temp, and that ESR at 80ºC is ~0.8 x ESR at room temperature.

Frequency Response

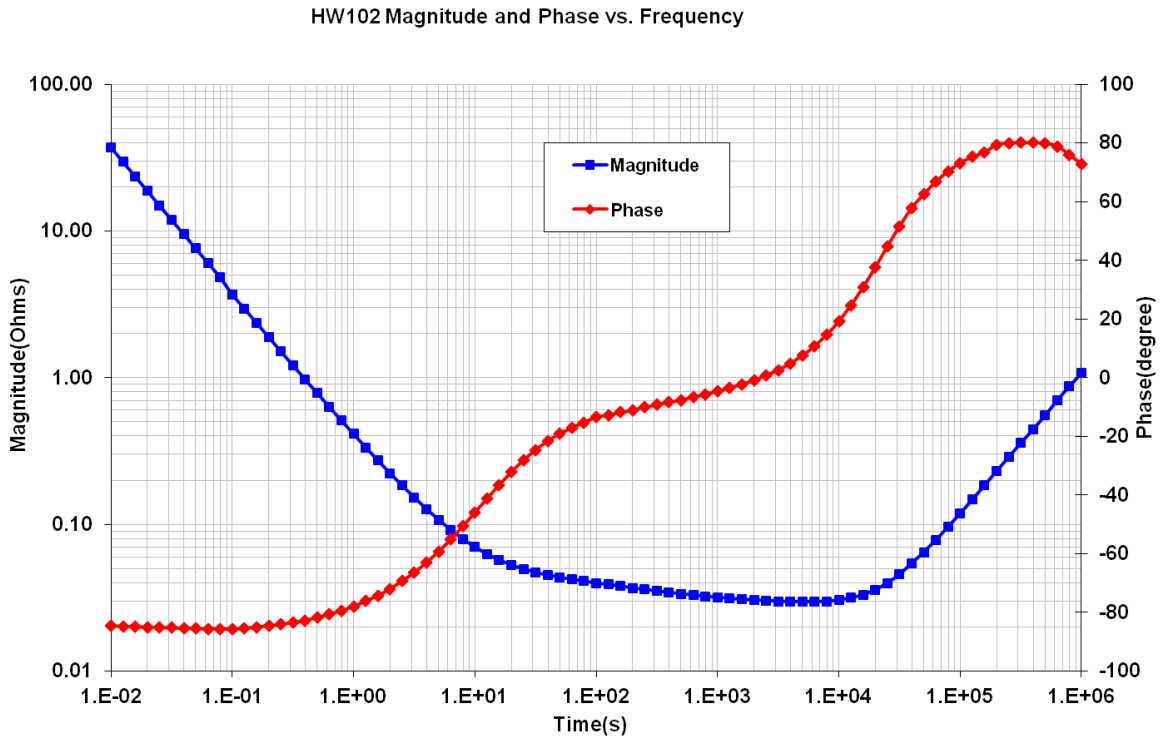

Fig 8: Frequency Response of Impedance (biased at 2.7V with a 50mV test signal)

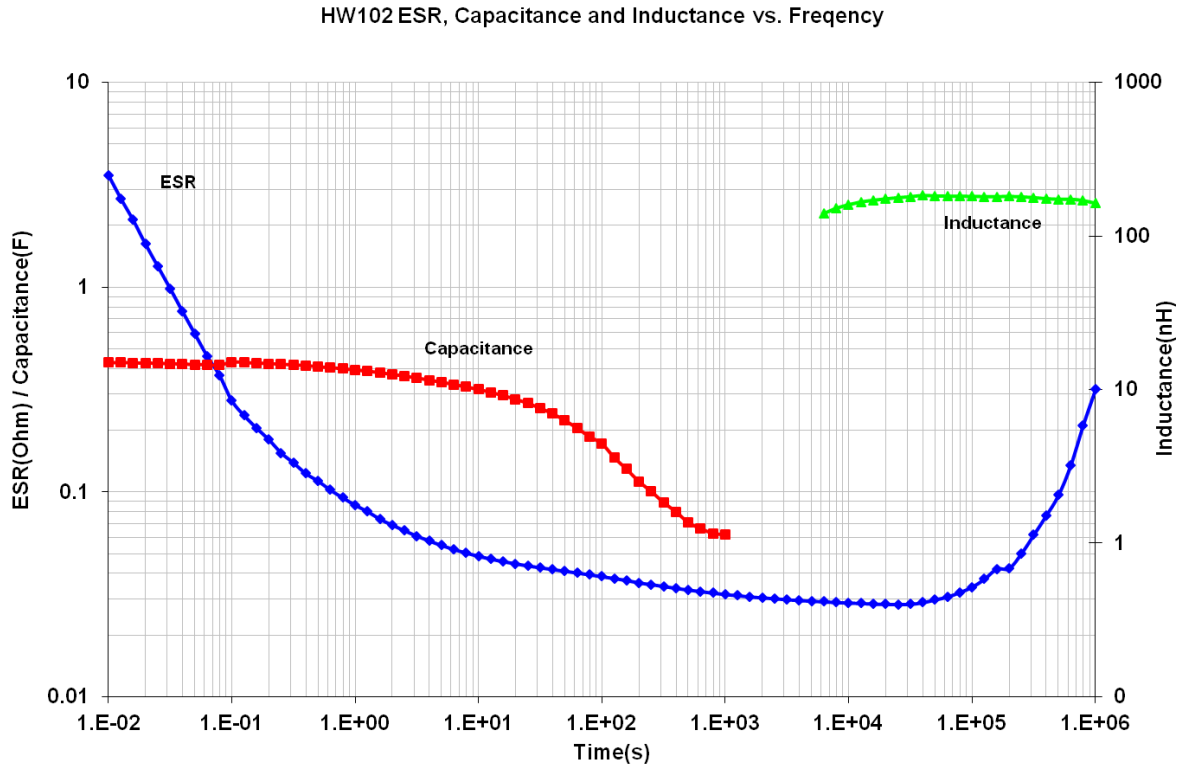

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 10 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

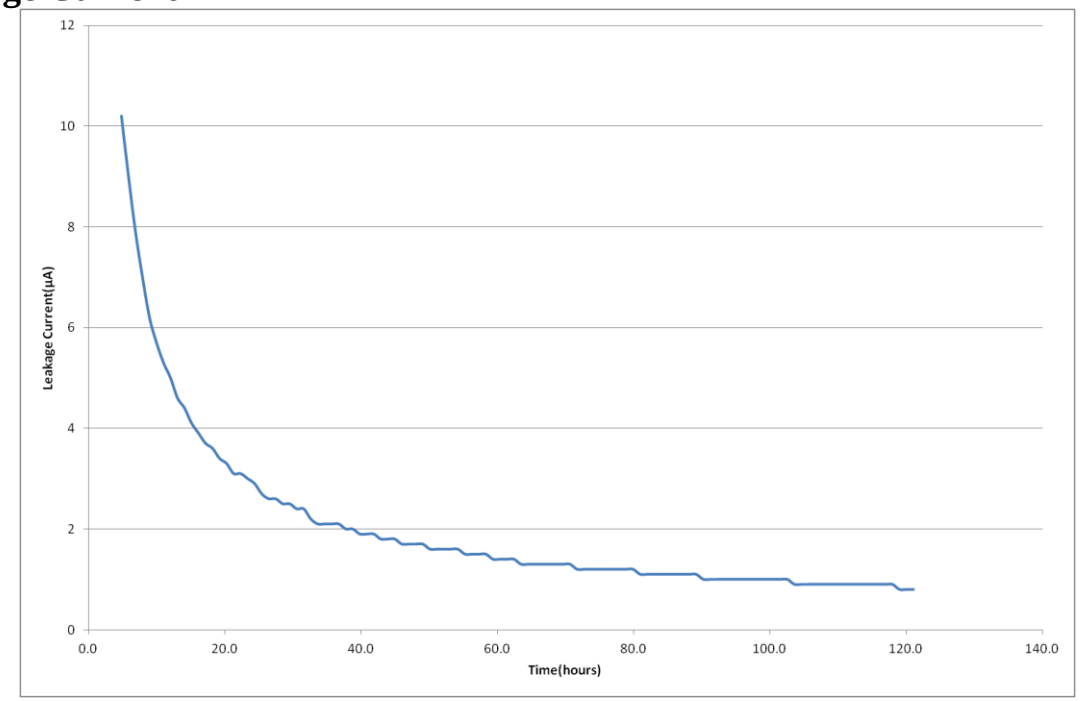

Fig 10: Leakage Current

Fig 10 shows the leakage current for HW102 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

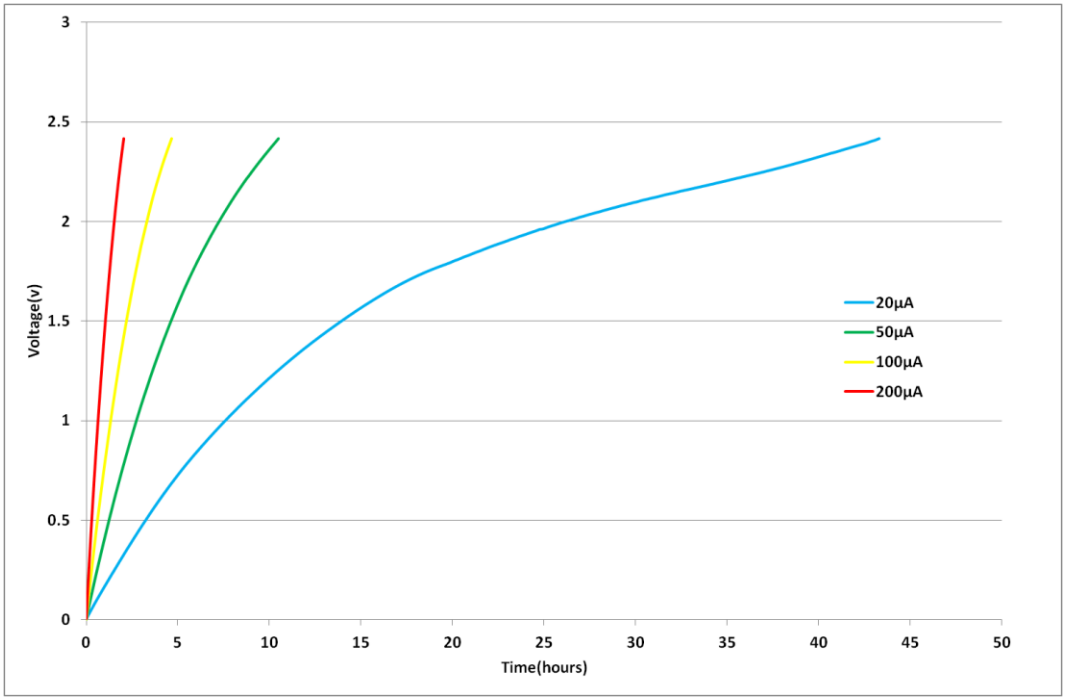

Fig 11: Charging an HW102 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 0.4F x 2.4V / 0.00002A = 13.3hrs to charge a 0.4 F supercapacitor to 2.4V at 20µA, but Fig 11 shows it took 45hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

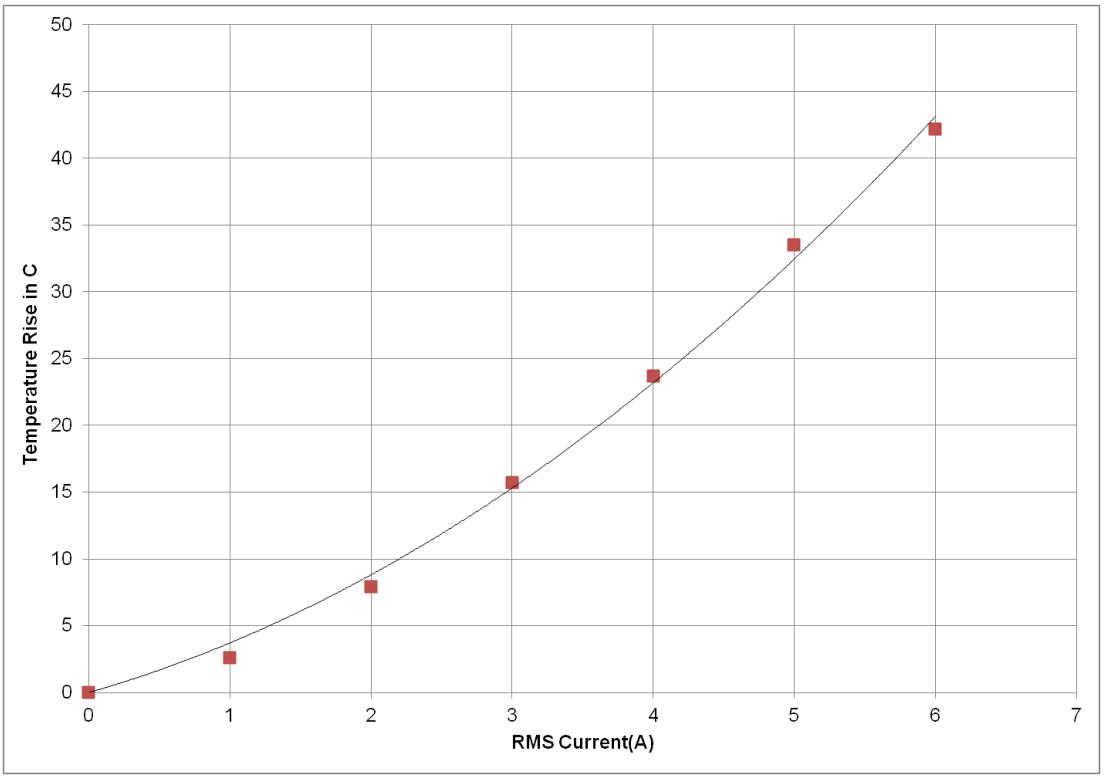

Fig 12: Temperature rise in HW202 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 4.6A, which causes a 30°C temperature increase.

CAP-XX Supercapacitors Product Guide

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HW103 / HW203 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HW103 is a single cell supercapacitor. The HW203 is a dual cell supercapacitor with two HW103 cells in series, so HW203 capacitance = Capacitance of HW103/2 and HW203 ESR = 2 x HW103 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HW103		0		2.9	V
		HW203				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HW103		0		2.75	V
		HW203		0		5.5	
Capacitance	C	HW103	DC, 23°C	800	1000	1200	mF
		HW203		400	500	600	
ESR	ESR	HW103	DC, 23°C		40	48	mΩ
		HW203			75	90	
Leakage Current	I_L		2.75V, 23°C 120hrs		1	2	µA
RMS Current	I_{RMS}		23°C			6	A
Peak Current[1]	I_P		23°C			30	A

[1]Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HW103F	**1.7mm**	No adhesive tape on underside of the supercapacitor	**HW103G**	**1.8mm**	Adhesive tape on underside, release tape removed
HW203F	**3.4mm**		**HW203G**	**3.5mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

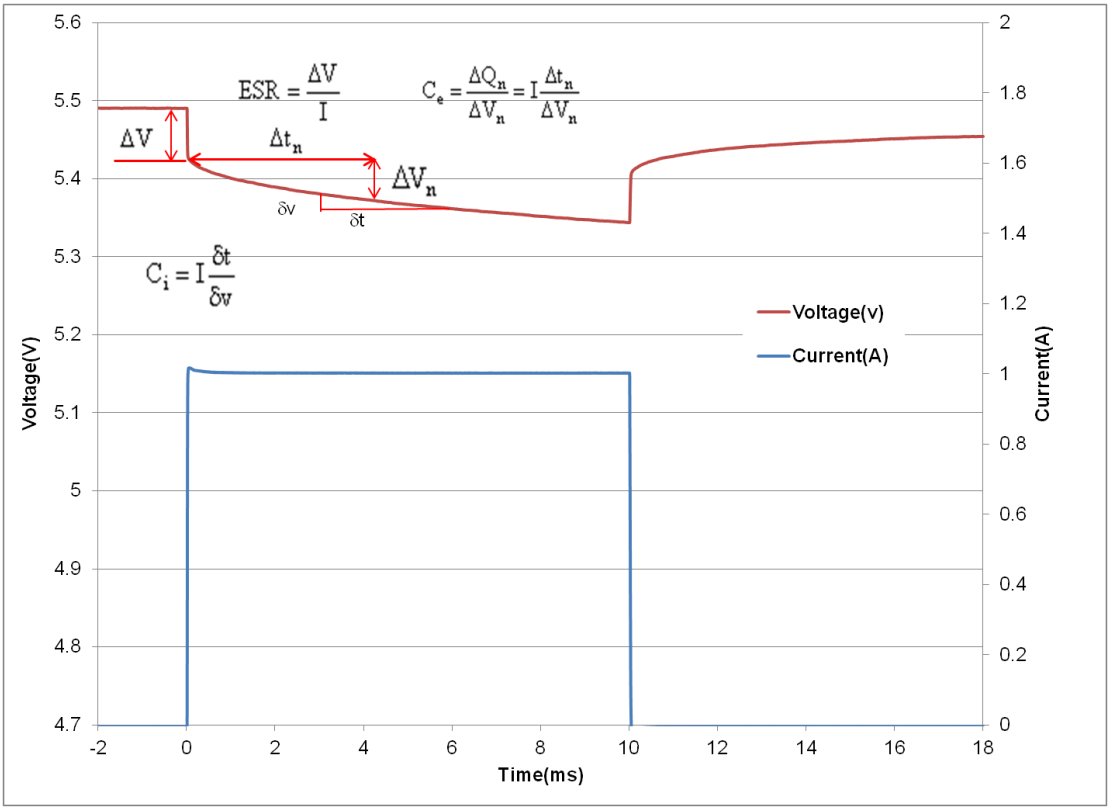

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HW203

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.490V-5.435V)/1A = 55mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I \times \Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.435 V – 5.389V) = 46mV. Therefore Ce(2ms) = 1A x 2ms/46mV = 43.5mF. After 10ms, the voltage drop = 5.435 V – 5.344V = 91mV. Therefore Ce(10ms) = 1 A x 10ms/91mV = 110mF. The DC capacitance of an HW203 = 0.5 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

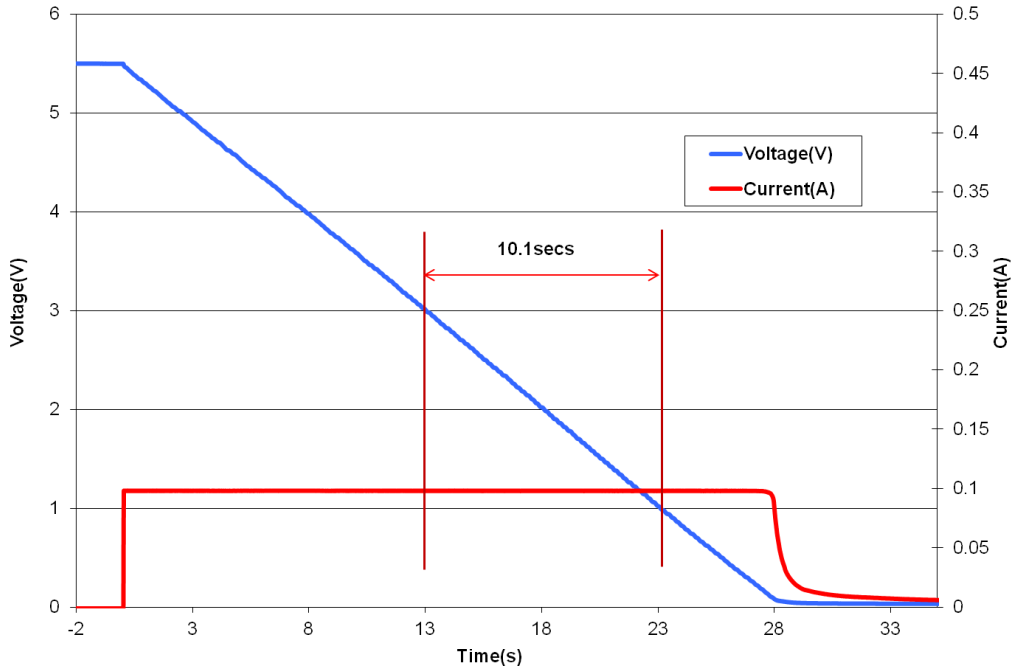

Fig 2: Measurement of DC Capacitance for an HW203

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 10.1s /2V = 505mF, which is well within the 500mF +/- 20% tolerance for an HW203 cell.

Measurement of ESR

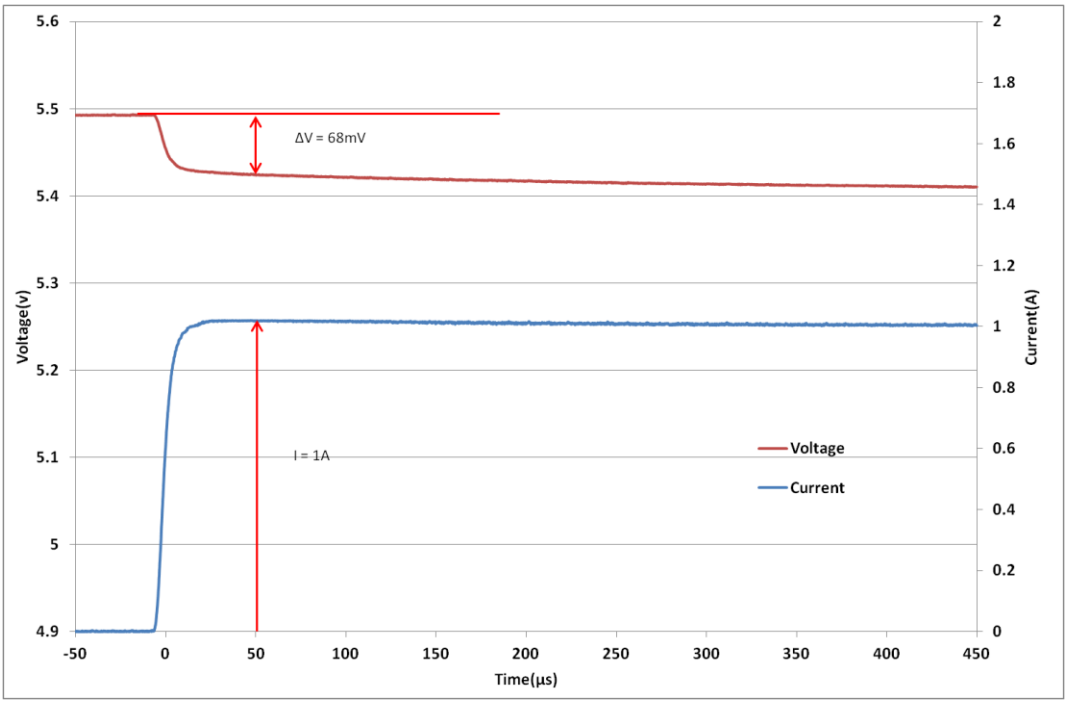

Fig 3: Measurement of ESR for an HW203

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 68mV/1A = 68mΩ.

Effective Capacitance

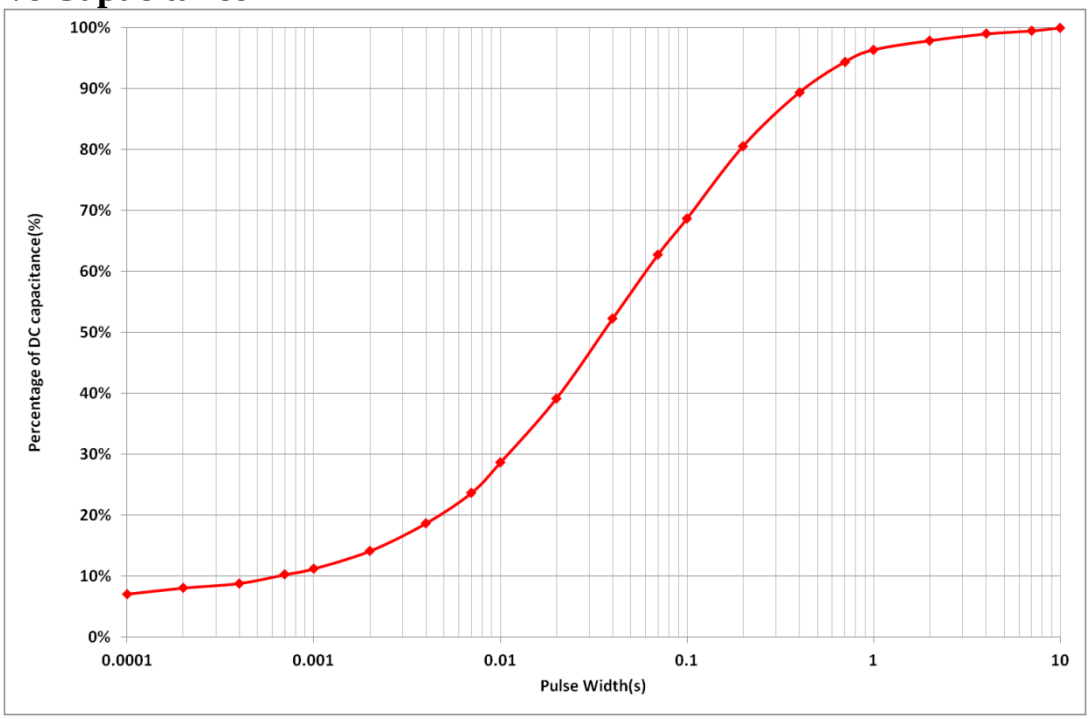

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HW103, HW203 @ 23°C. This shows that for a 1msec PW, you will measure 11% of DC capacitance or 110mF for an HW103 or 55mF for an HW203. At 10msecs you will measure 29% of the DC capacitance, and at 100msecs you will measure 69% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10msecs, then you would use the Ceff(10msecs) = 29% of DC capacitance = 145mF for an HW203, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 70mΩ + 1A x 10ms / 145mF = 139mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

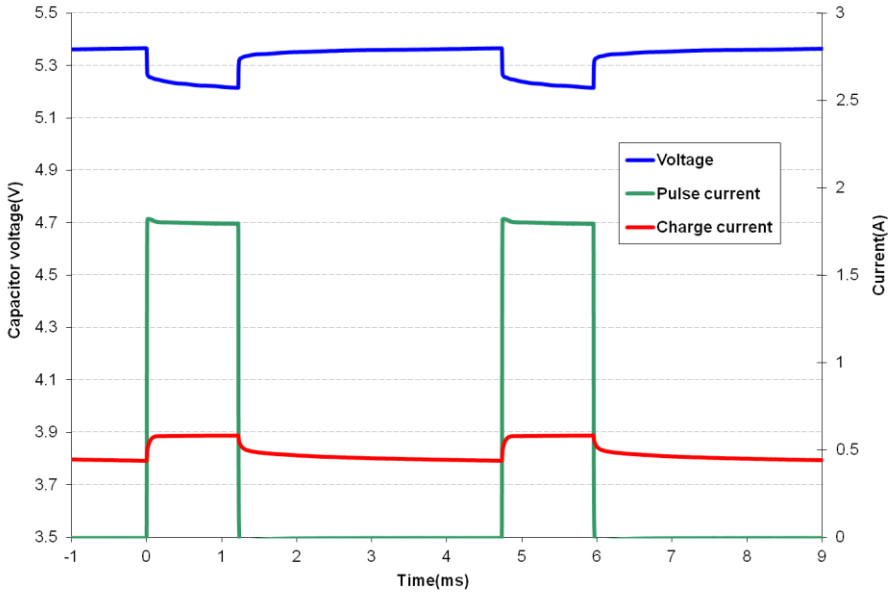

Fig 5 shows that the HW203 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 55mF coupled with the low ESR supports this pulse train with only ~150mV droop in the supply rail.

Fig 5: HW203 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

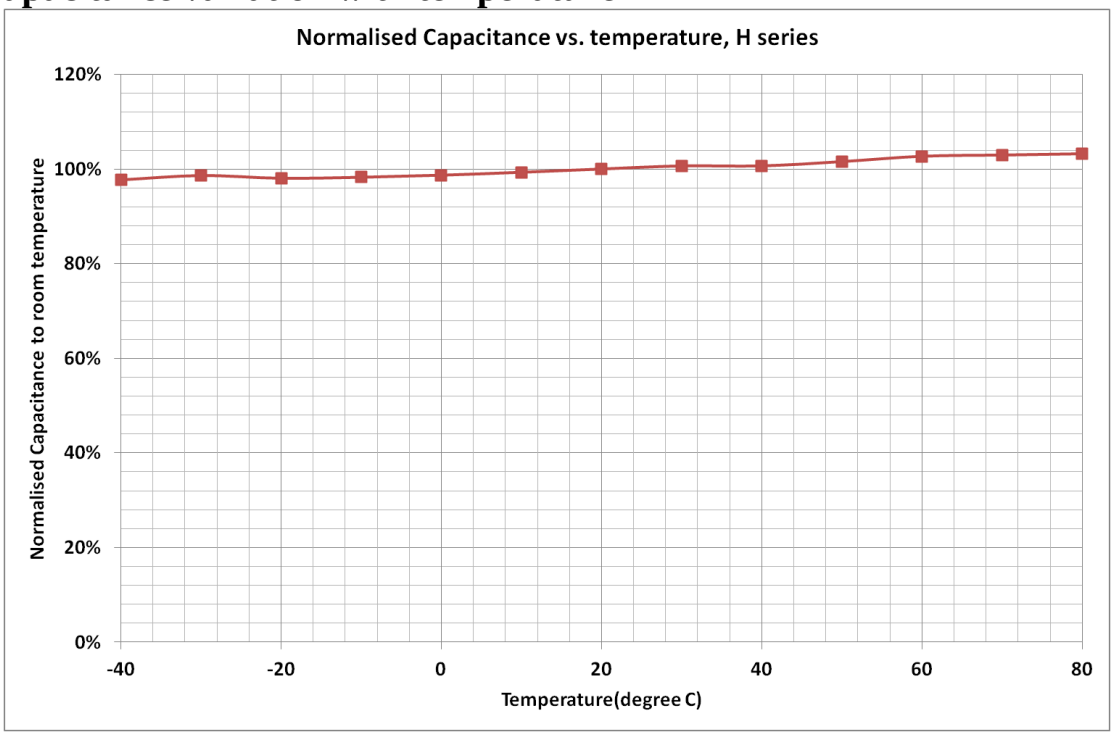

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

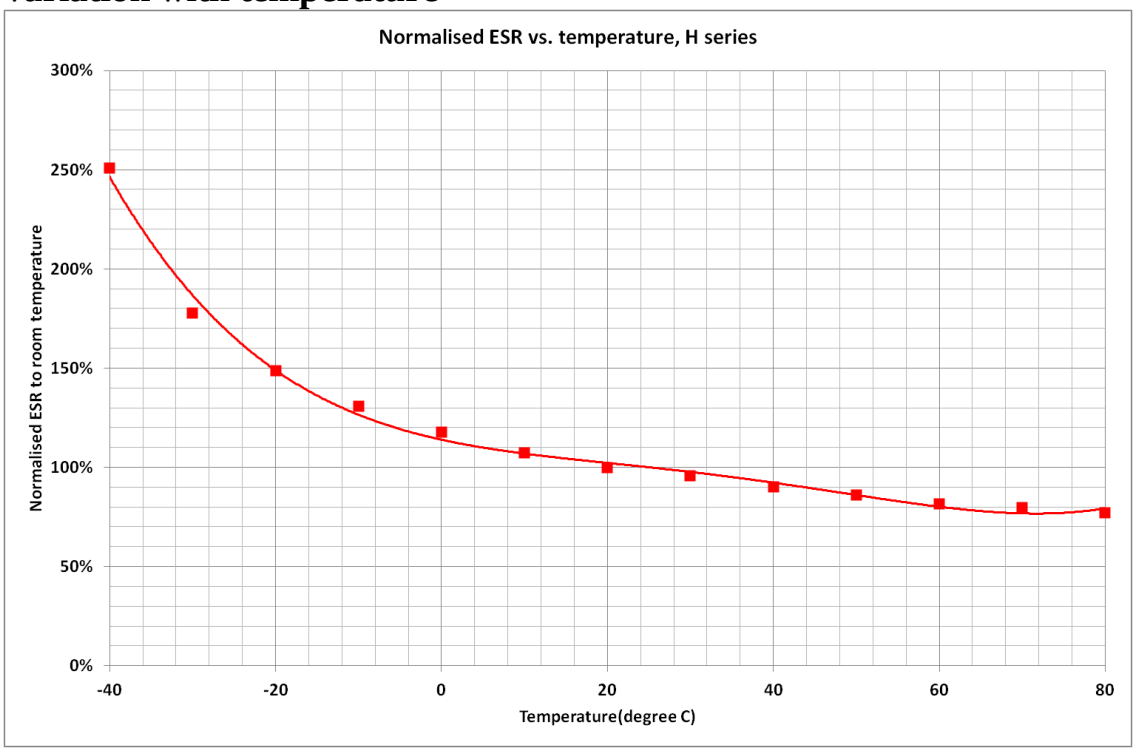

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.5 x ESR at room temp, and that ESR at 80ºC is ~0.8 x ESR at room temperature.

Frequency Response

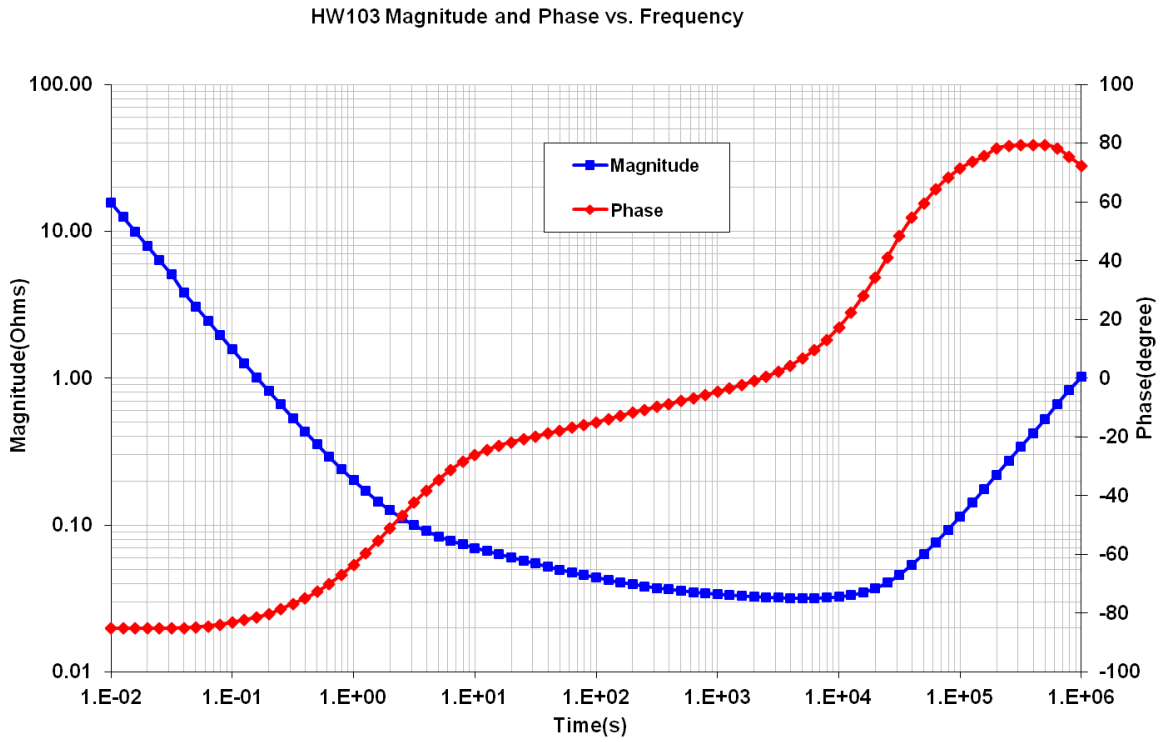

Fig 8: Frequency Response of Impedance (biased at 2.7V with a 50mV test signal)

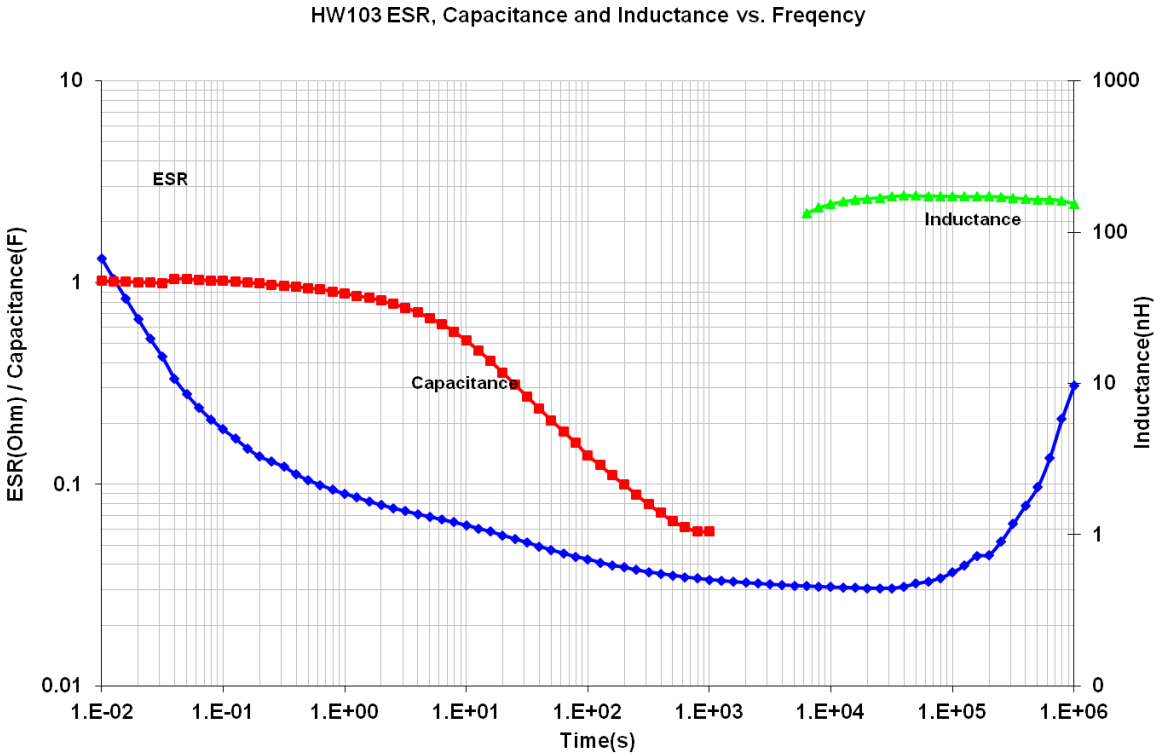

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 3 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

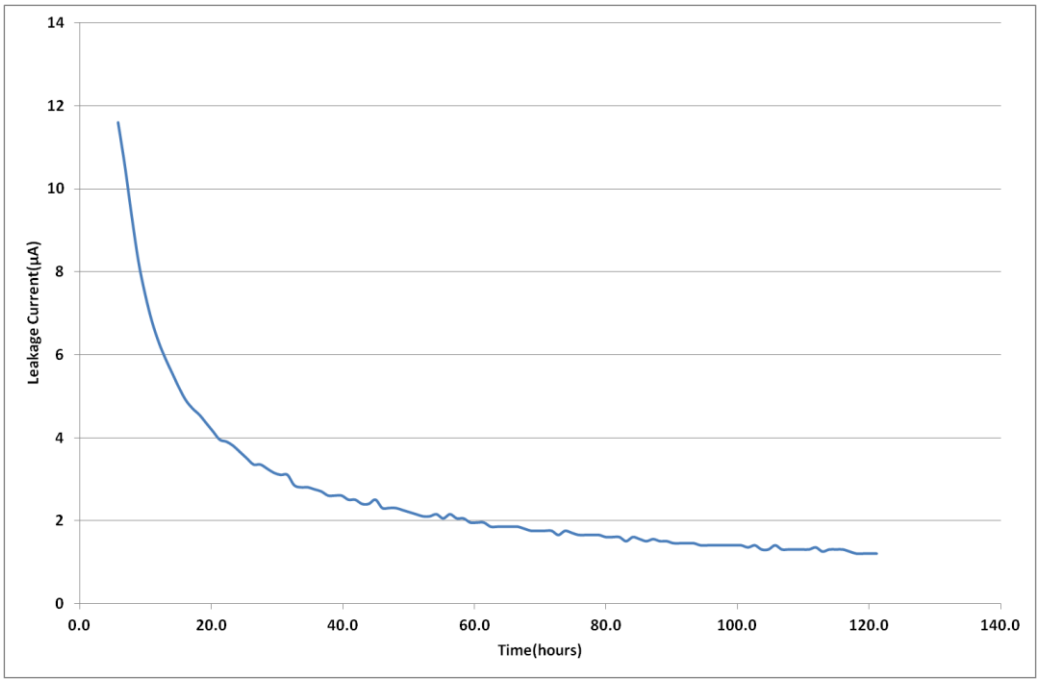

Fig 10: Leakage Current

Fig 10 shows the leakage current for HW103 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

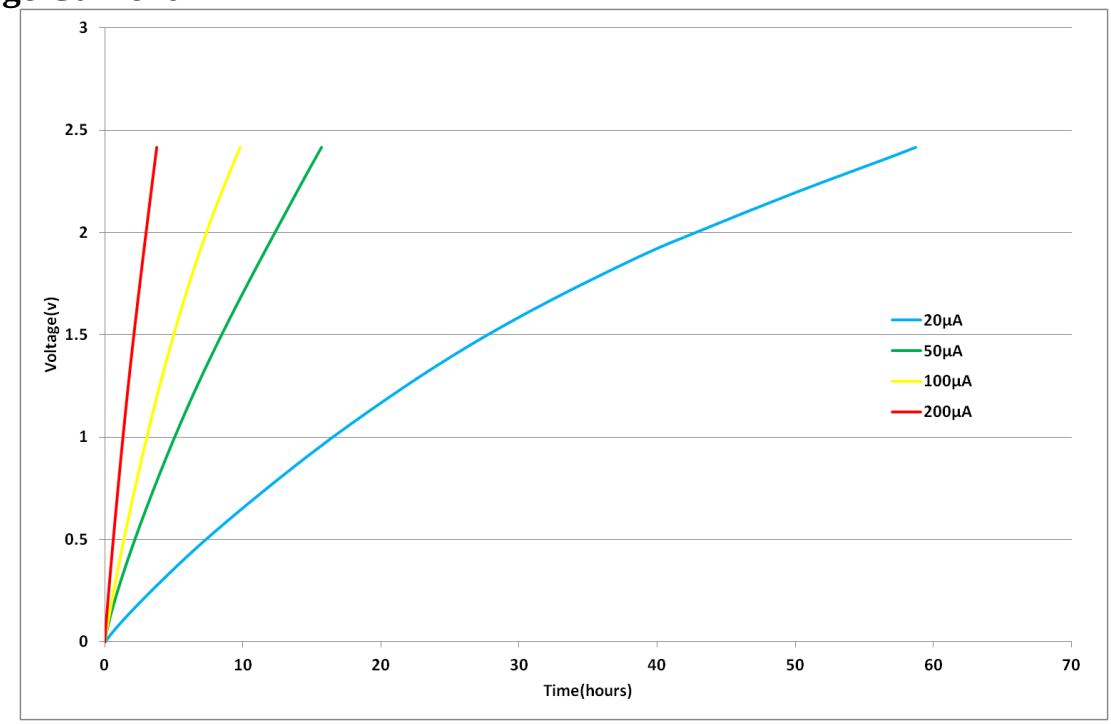

Fig 11: Charging an HW103 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 1 F x 2.4V / 0.00002A = 33.3hrs to charge a 1 F supercapacitor to 2.4V at 20µA, but Fig 11 shows it took 60hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

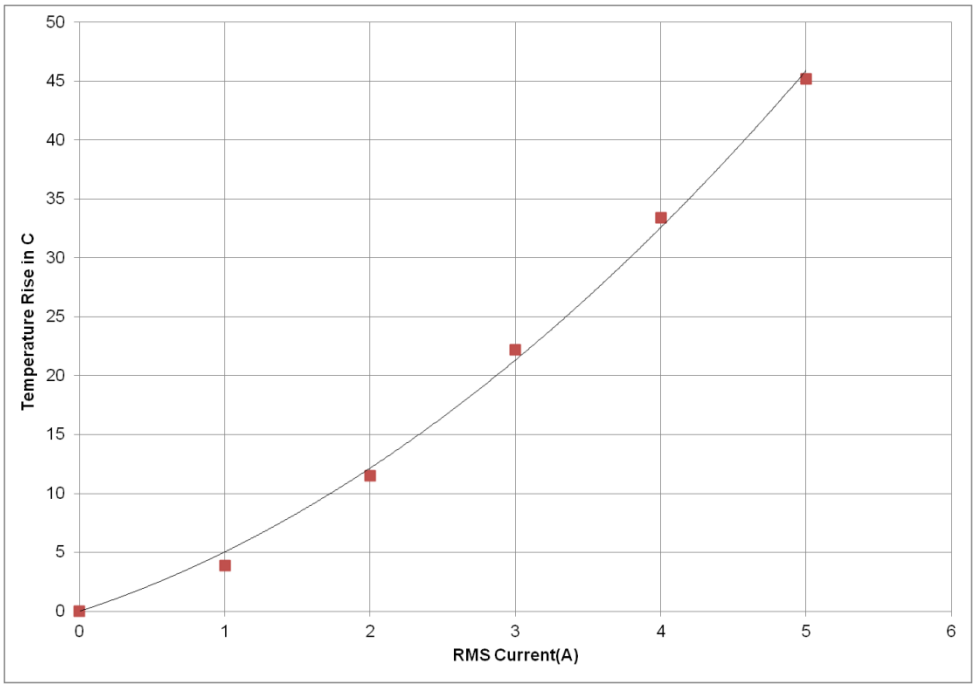

Fig 12: Temperature rise in HW203 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 3.6A, which causes a 30°C temperature increase.

CAP-XX Supercapacitors Product Guide

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Refer to the CAP-XX Supercapacitors Product Guide for information on endurance and shelf life, transportation and storage, assembly and soldering, safety and RoHS/EREACH certification.

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ACN 077 060 872

HW109 / HW209 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HW109 is a single cell supercapacitor. The HW209 is a dual cell supercapacitor with two HW109 cells in series, so HW209 capacitance = Capacitance of HW109/2 and HW209 ESR = 2 x HW109 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HW109		0		2.9	V
		HW209				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HW109		0		2.75	V
		HW209		0		5.5	
Capacitance	C	HW109	DC, 23°C	240	300	360	mF
		HW209		120	150	180	
ESR	ESR	HW109	DC, 23°C		50	60	mΩ
		HW209			100	120	
Leakage Current	I_L		2.75V, 23°C 120hrs		1	2	µA
RMS Current	I_{RMS}		23°C			4	A
Peak Current[1]	I_P		23°C			30	A

[1]Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HW109F	**1.0mm**	No adhesive tape on underside of the supercapacitor	**HW109G**	**1.1mm**	Adhesive tape on underside, release tape removed
HW209F	**2.1mm**		**HW209G**	**2.2mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

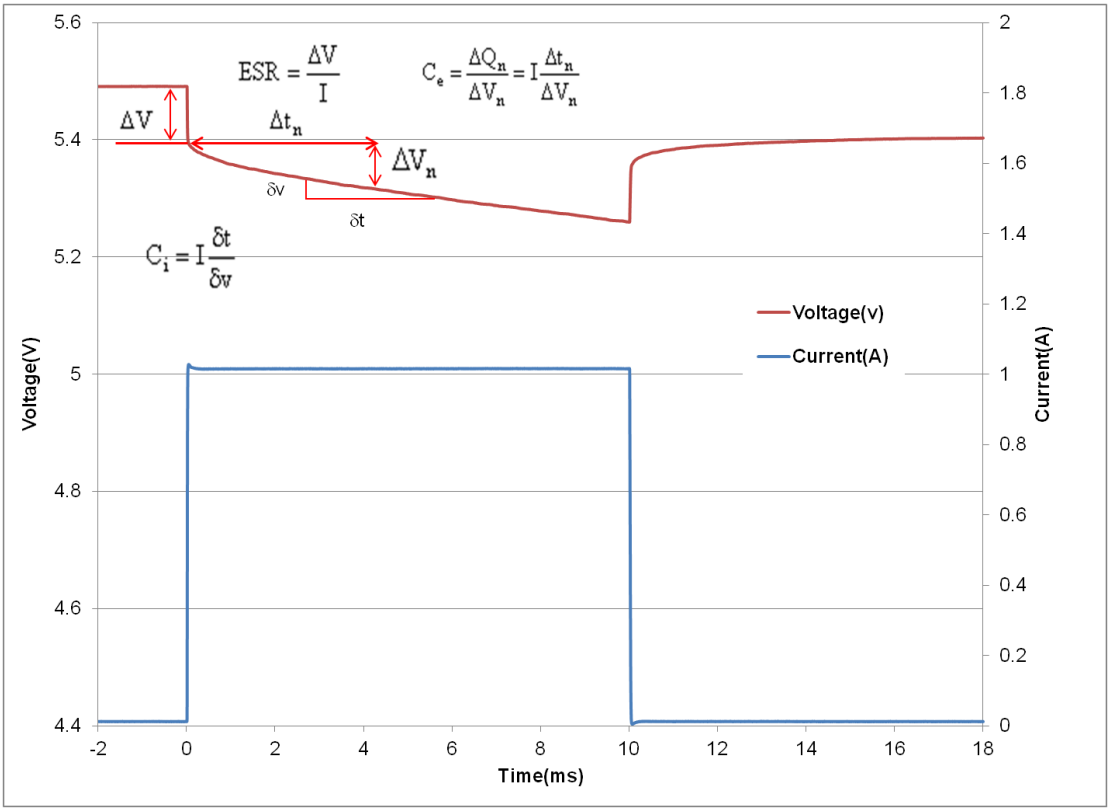

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HW209

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.491V-5.403V)/1A = 117mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I \times \Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.403 V – 5.342V) = 61mV. Therefore Ce(2ms) = 1A x 2ms/61mV = 32.8mF. After 10ms, the voltage drop = 5.403 V – 5.261V = 142mV. Therefore Ce(10ms) = 1 A x 10ms/142mV = 70.4mF. The DC capacitance of an HW209 = 0.15 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

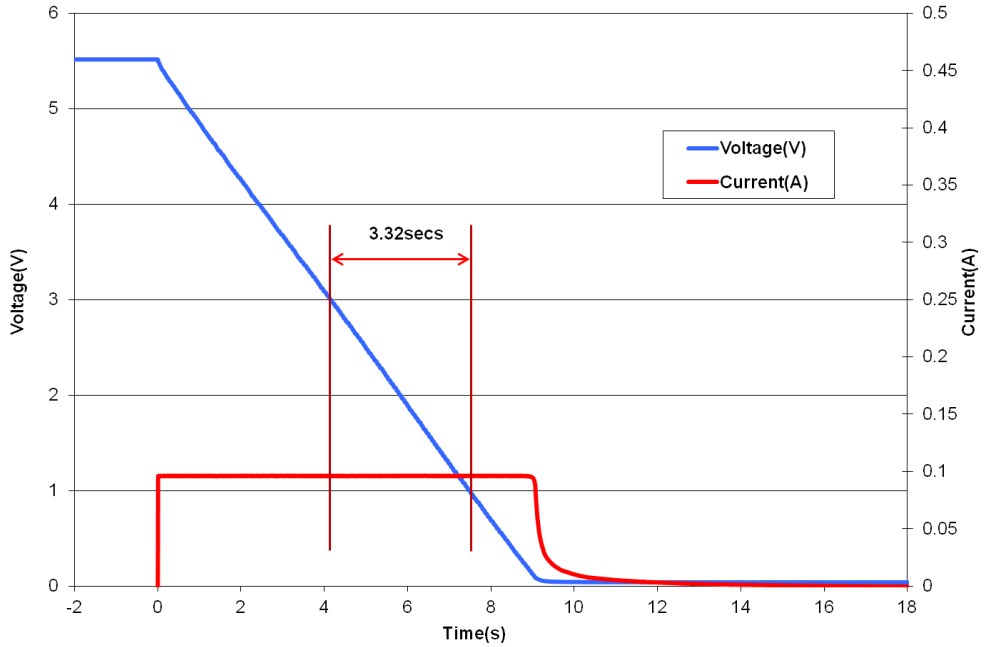

Fig 2: Measurement of DC Capacitance for an HW209

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 3.32s /2V = 166mF, which is well within the 150mF +/- 20% tolerance for an HW209 cell.

Measurement of ESR

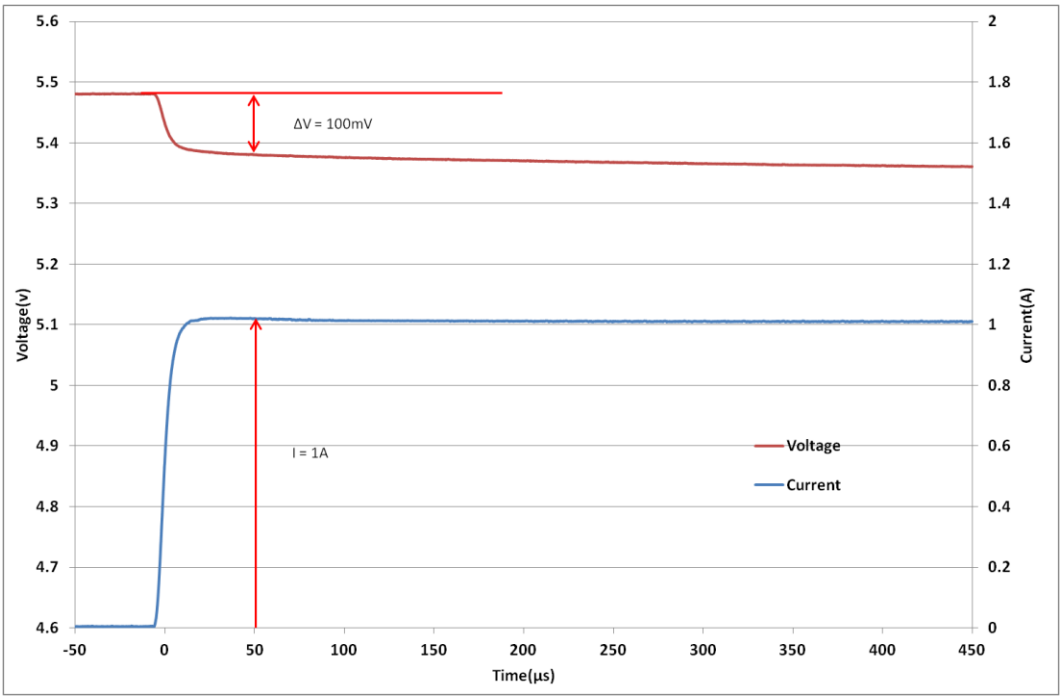

Fig 3: Measurement of ESR for an HW209

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 100mV/1.A = 100mΩ.

Effective Capacitance

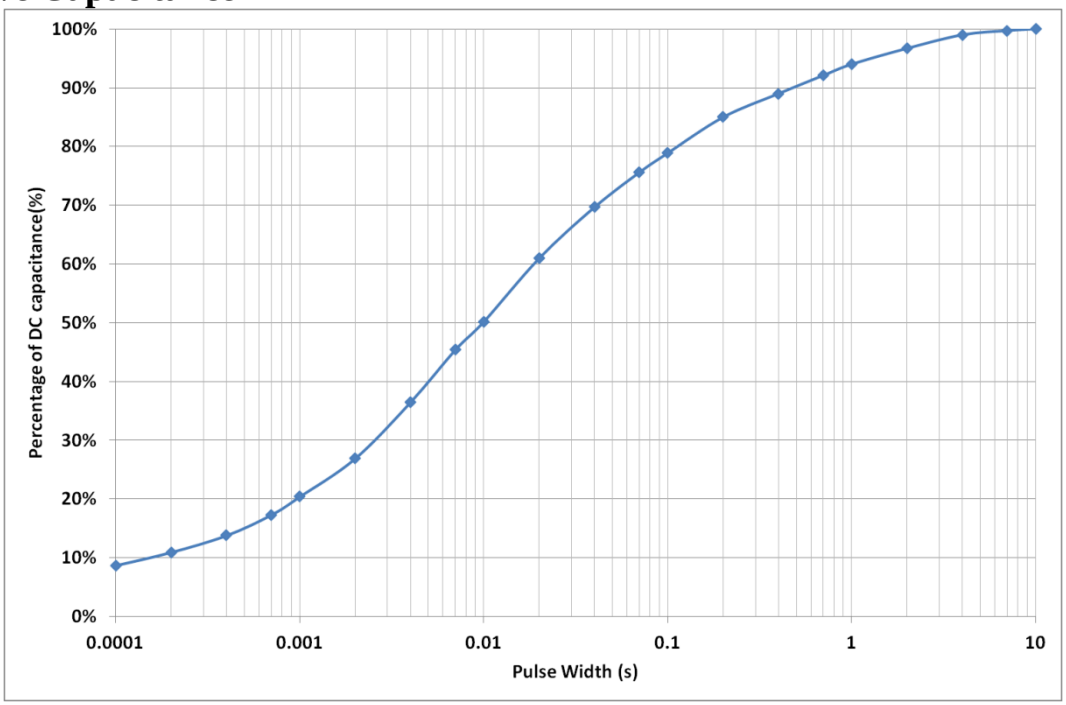

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HW109, HW209 @ 23°C. This shows that for a 1msec PW, you will measure 20.4% of DC capacitance or 61.2mF for an HW109 or 30.6mF for an HW209. At 10msecs you will measure 50% of the DC capacitance, and at 100msecs you will measure 79% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10msecs, then you would use the Ceff(10msecs) = 50% of DC capacitance = 75mF for an HW209, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 90mΩ + 1A x 10ms / 75mF = 223mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

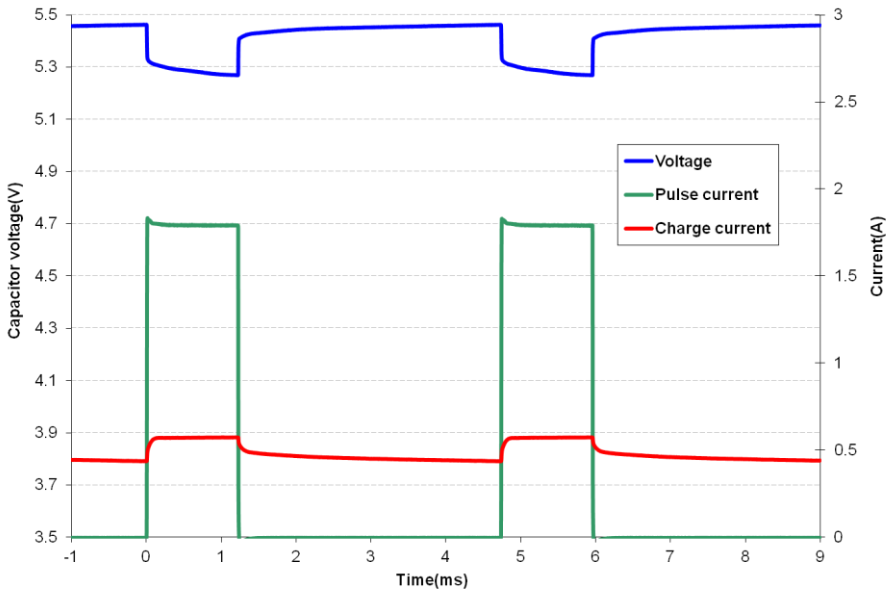

Fig 5 shows that the HW209 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 30.6mF coupled with the low ESR supports this pulse train with only ~190mV droop in the supply rail.

Fig 5: HW209 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

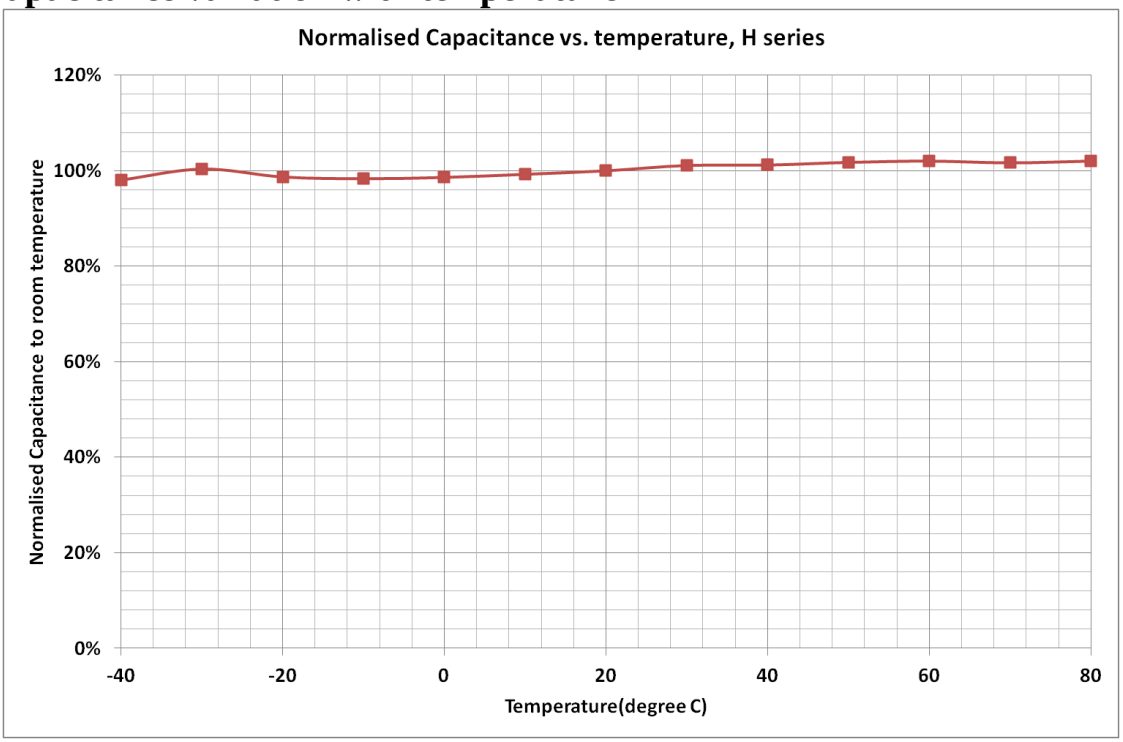

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

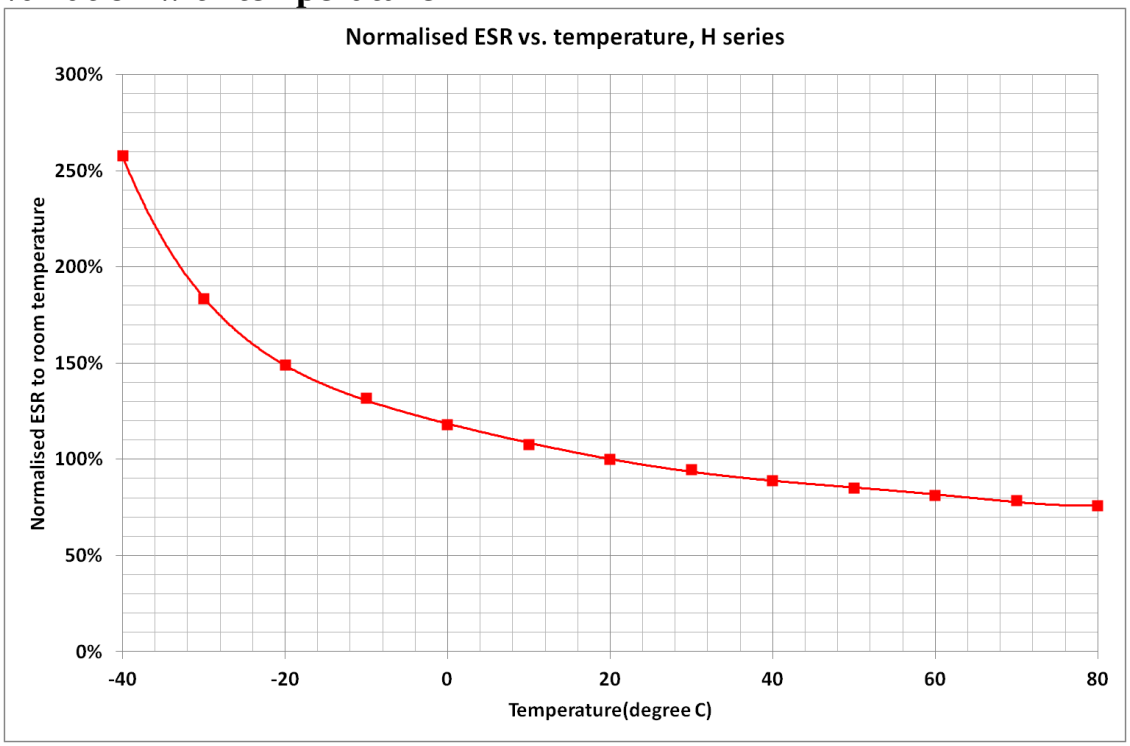

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.6 x ESR at room temp, and that ESR at 80ºC is ~0.8 x ESR at room temperature.

Frequency Response

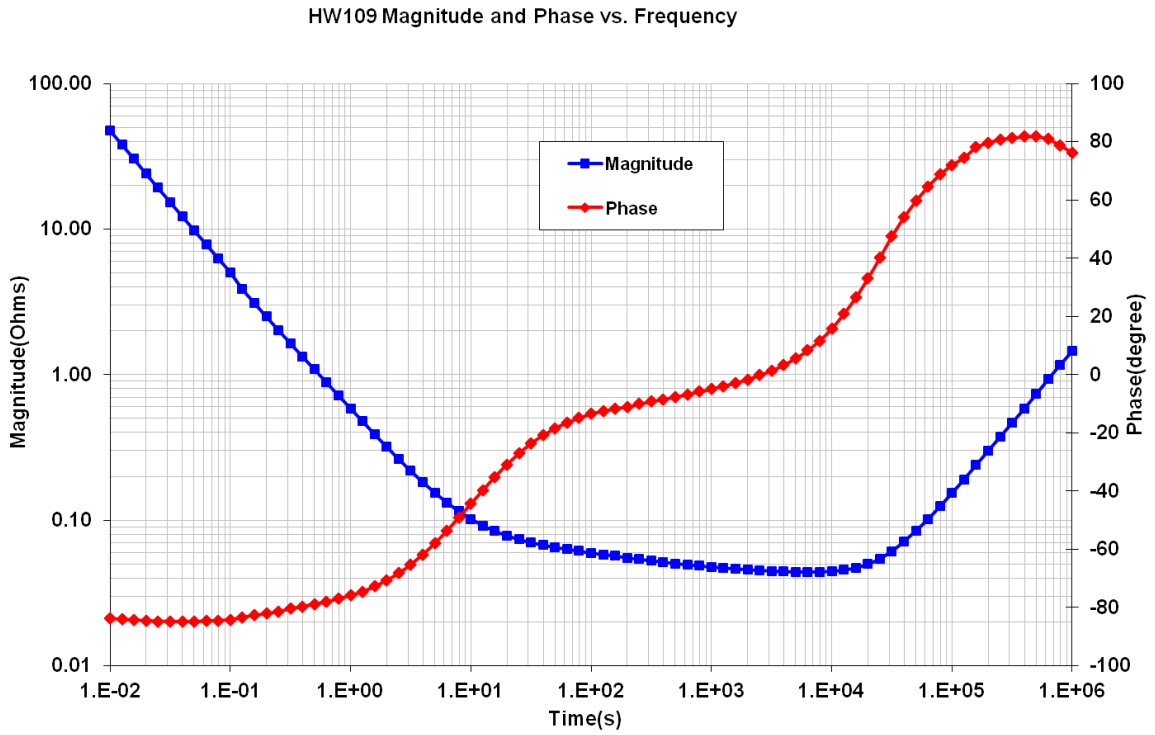

Fig 8: Frequency Response of Impedance (biased at 2.7V with a 50mV test signal)

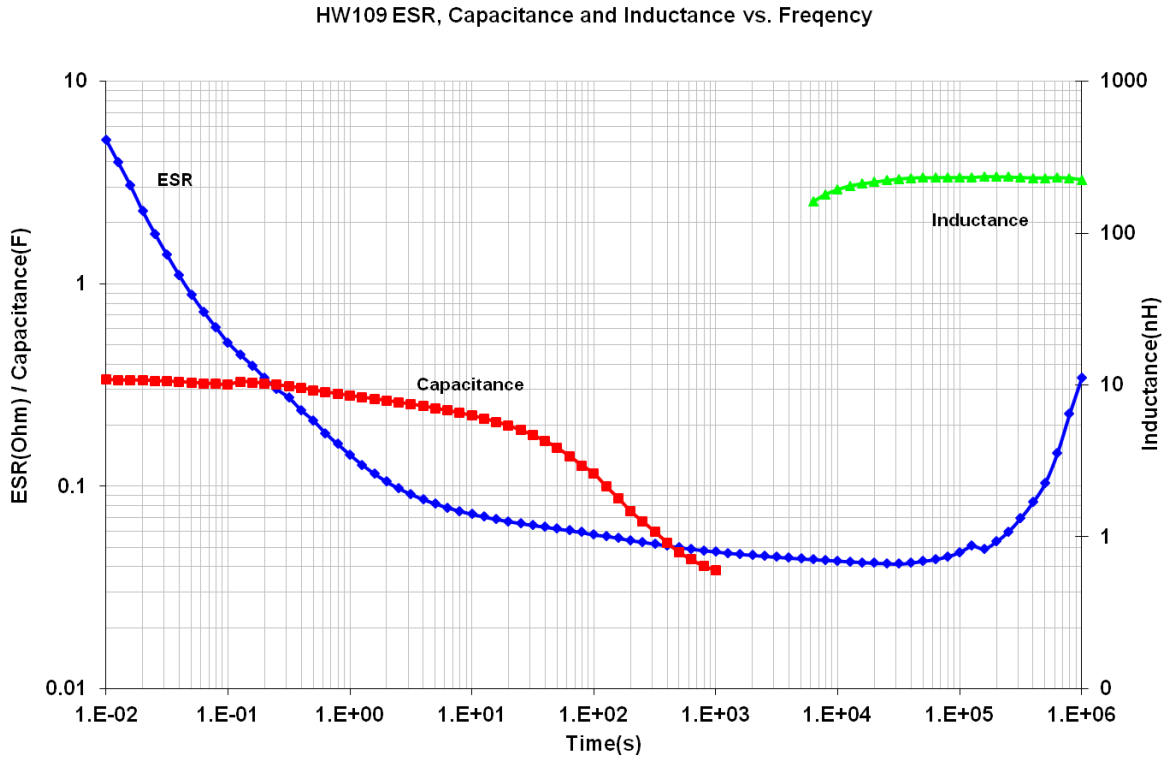

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 7 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

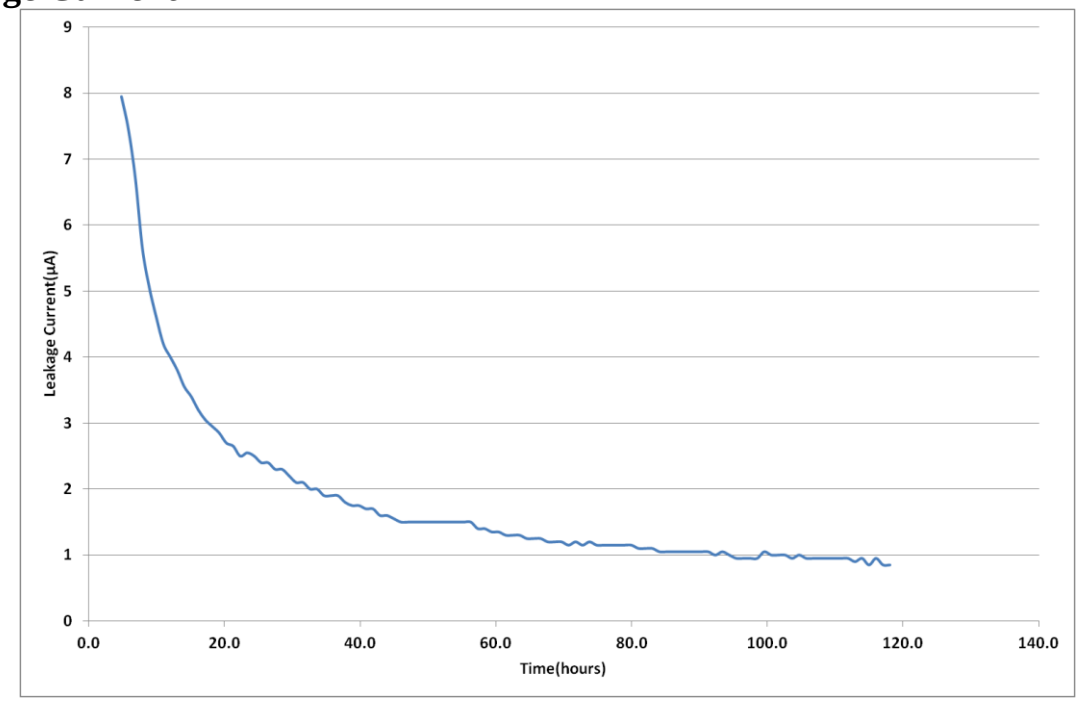

Fig 10: Leakage Current

Fig 10 shows the leakage current for HW109 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

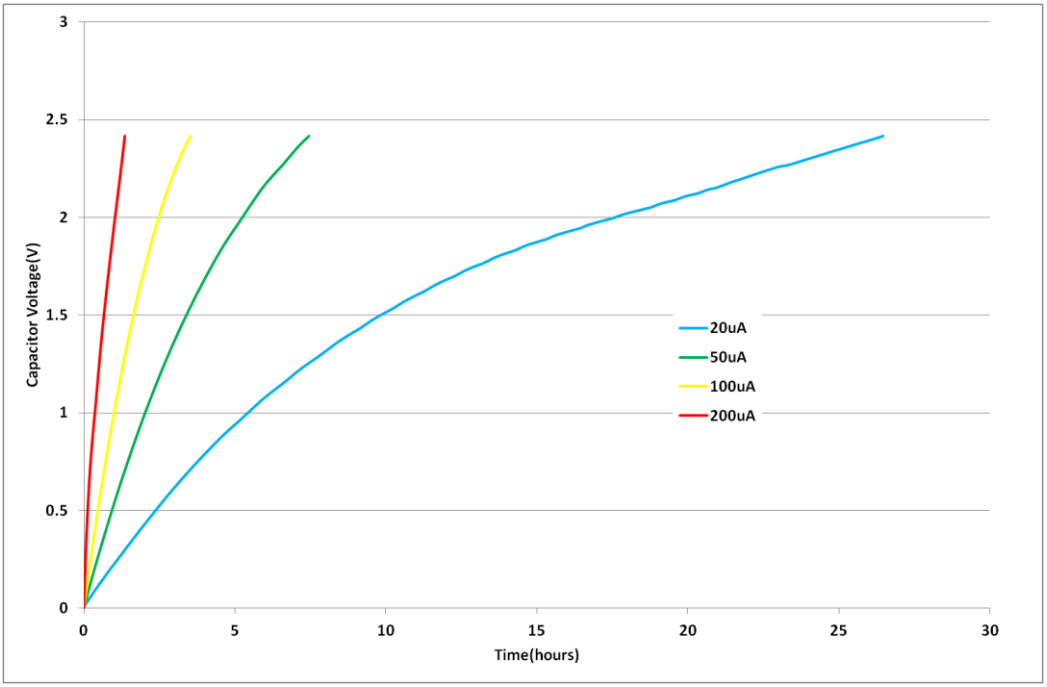

Fig 11: Charging an HW109 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 0.3F x 2.4V / 0.00002A = 10hrs to charge a 0.3 F supercapacitor to 2.4V at 20µA, but Fig 11 shows it took 27hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

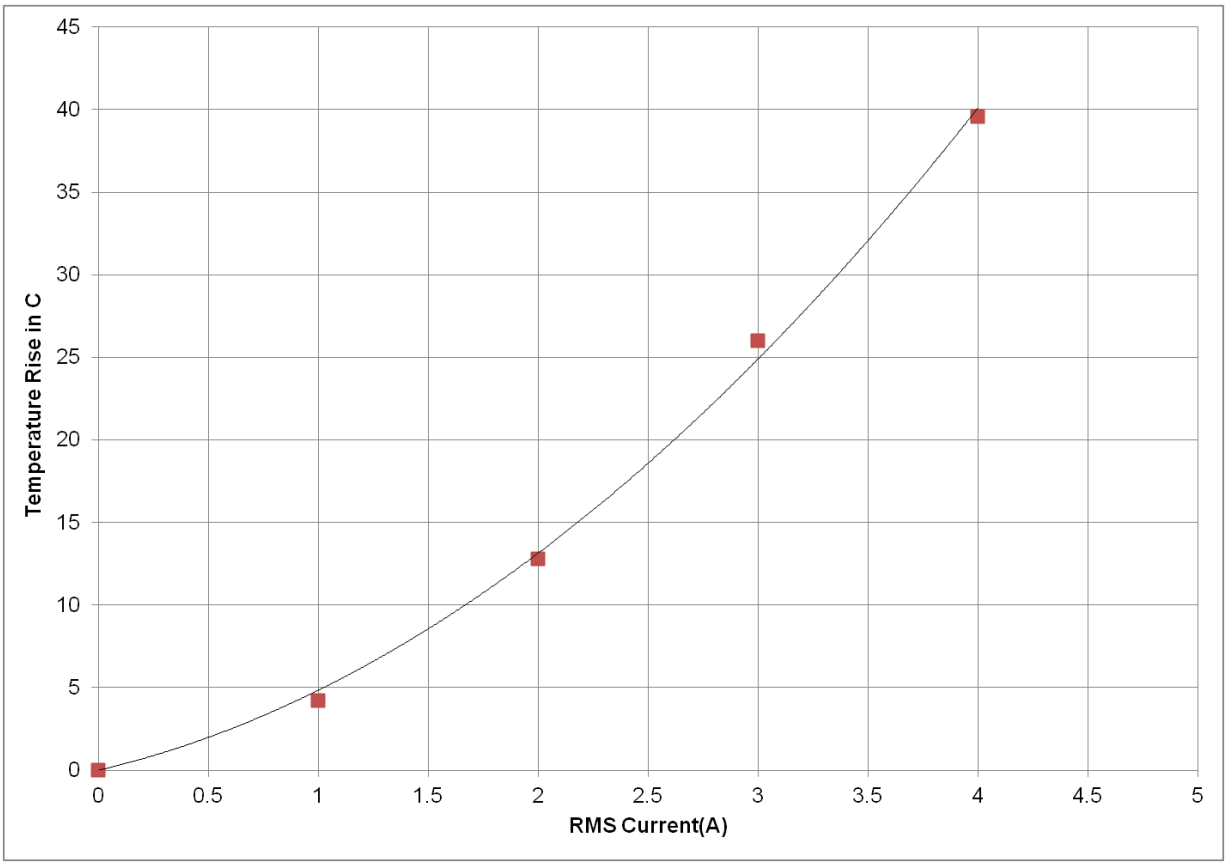

Fig 12: Temperature rise in HW209 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 3.3A, which causes a 30°C temperature increase.

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