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HS103 / HS203 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HS103 is a single cell supercapacitor. The HS203 is a dual cell supercapacitor with two HS103 cells in series, so HS203 capacitance = Capacitance of HS103/2 and HS203 ESR = 2 x HS103 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HS103		0		2.9	V
		HS203				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HS103		0		2.75	V
		HS203		0		5.5	
Capacitance	C	HS103	DC, 23°C	400	500	600	mF
		HS203		200	250	300	
ESR	ESR	HS103	DC, 23°C		30	36	mΩ
		HS203			55	66	
Leakage Current	I_L		2.75V, 23°C 120hrs		1	2	µA
RMS Current	I_{RMS}		23°C			6	A
Peak Current[1]	I_P		23°C			30	A

[1] Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HS103F	**1.0mm**	No adhesive tape on underside of the supercapacitor	**HS103G**	**1.1 mm**	Adhesive tape on underside, release tape removed
HS203F	**2.1mm**		**HS203G**	**2.2mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

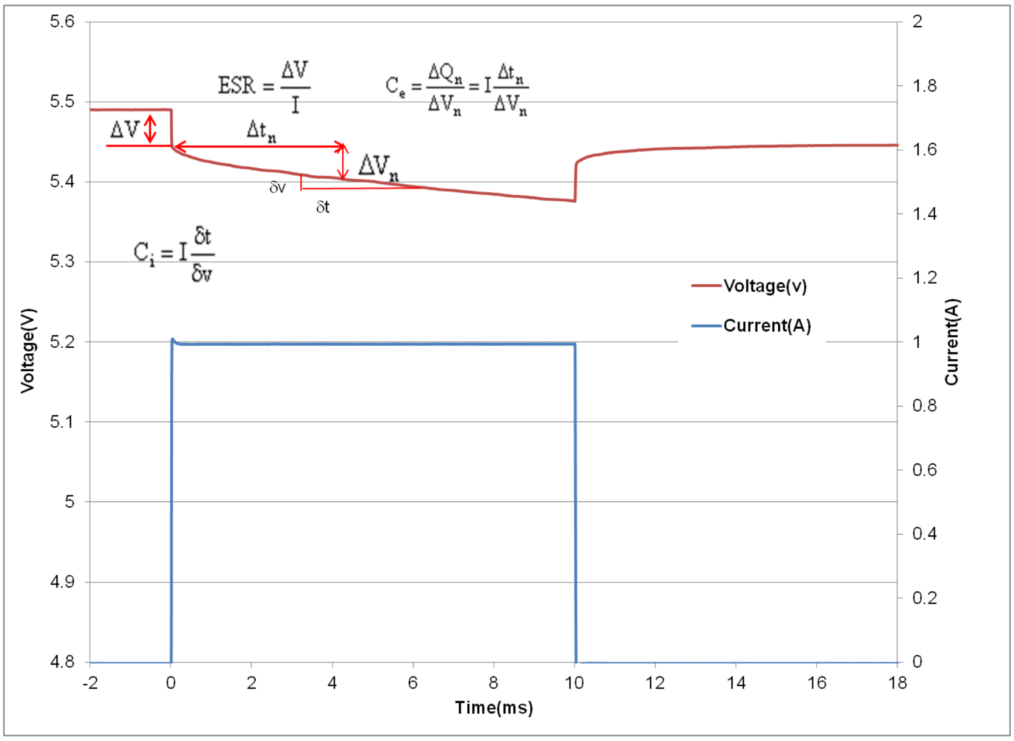

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HS203

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.49V – 5.45V)/1A = 40mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I$ x $\Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.45 V – 5.416V) = 34mV. Therefore Ce(2ms) = 1A x 2ms/34mV = 58.8mF. After 10ms, the voltage drop = 5.45 V – 5.376V = 74mV. Therefore Ce(10ms) = 1 A x 10ms/74mV = 135mF. The DC capacitance of an HS203 = 0.25 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

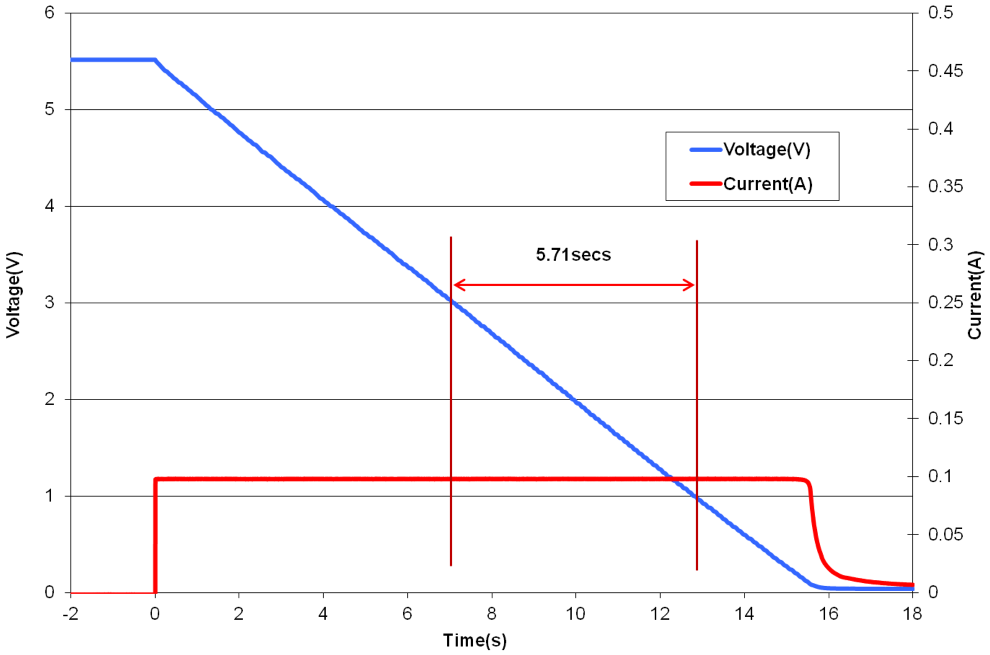

Fig 2: Measurement of DC Capacitance for an HS203

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 5.71s /2V = 285.5mF, which is well within the 0.25F +/- 20% tolerance for an HS203 cell.

Measurement of ESR

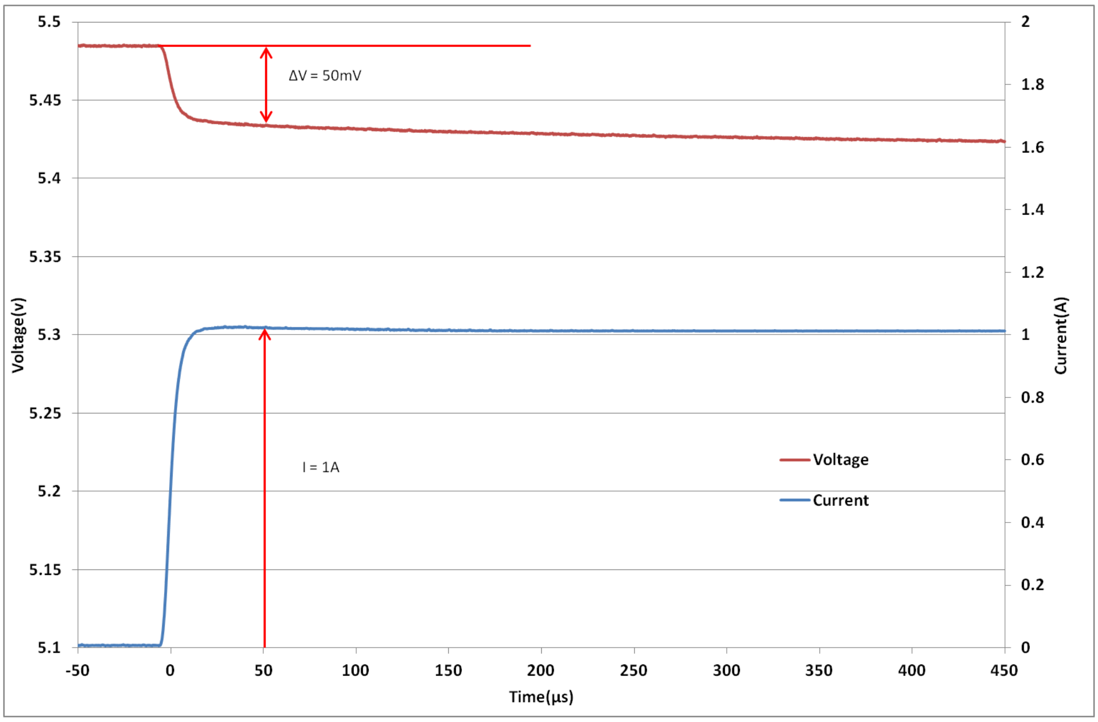

Fig 3: Measurement of ESR for an HS203

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 50mV/1.A = 50mΩ.

Effective Capacitance

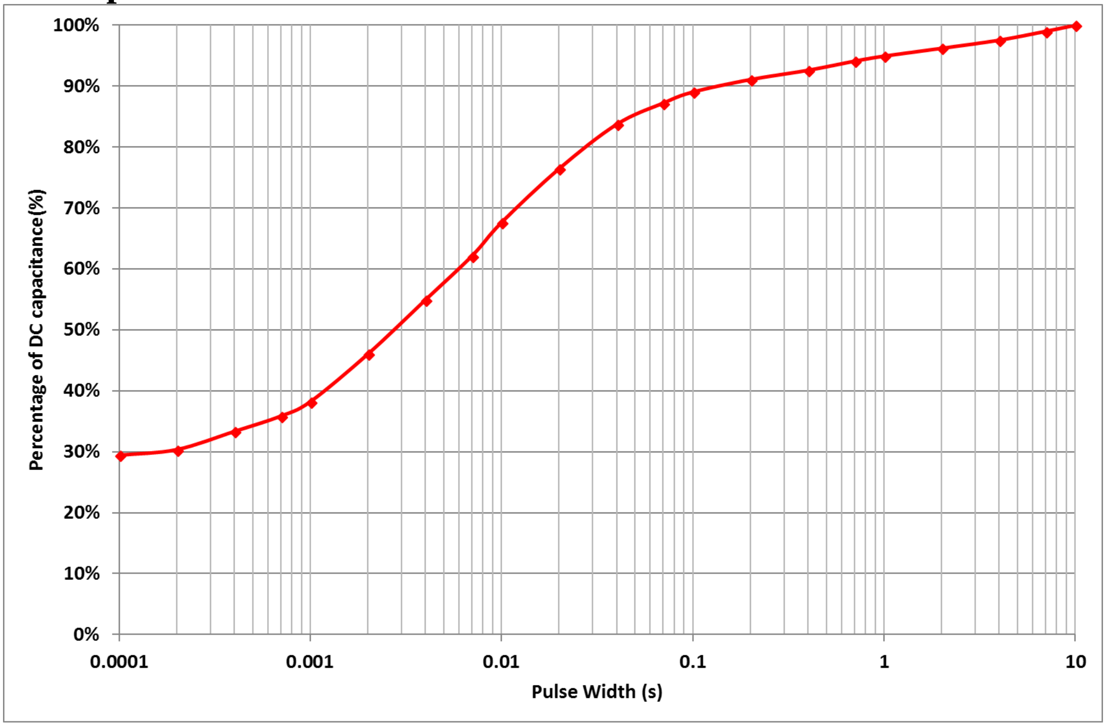

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HS103, HS203 @ 23°C. This shows that for a 1ms PW, you will measure 38% of DC capacitance or 190mF for an HS103 or 95mF for an HS203. At 10ms you will measure 67% of the DC capacitance, and at 100ms you will measure 89% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10ms, then you would use the Ceff(10ms) = 67% of DC capacitance = 167.5mF for an HS203, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 55mΩ + 1A x 10ms / 167.5mF = 115mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

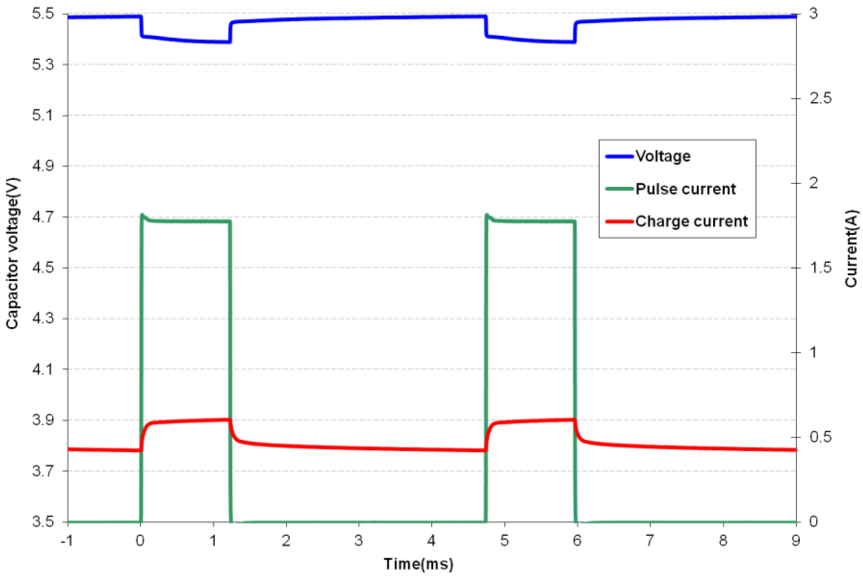

Fig 5: HS203 Pulse Response with GPRS Class 10 Pulse Train

Pulse Response

Fig 5 shows that the HS203 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 43.8mF coupled with the low ESR supports this pulse train with only ~100mV droop in the supply rail.

DC Capacitance variation with temperature

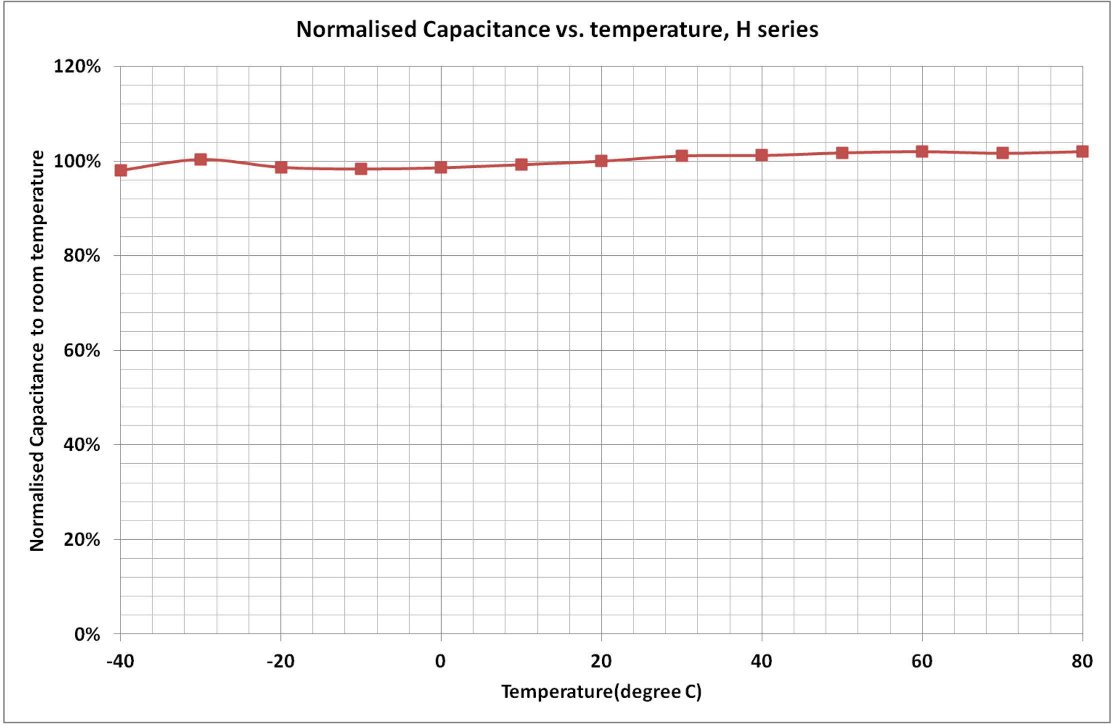

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

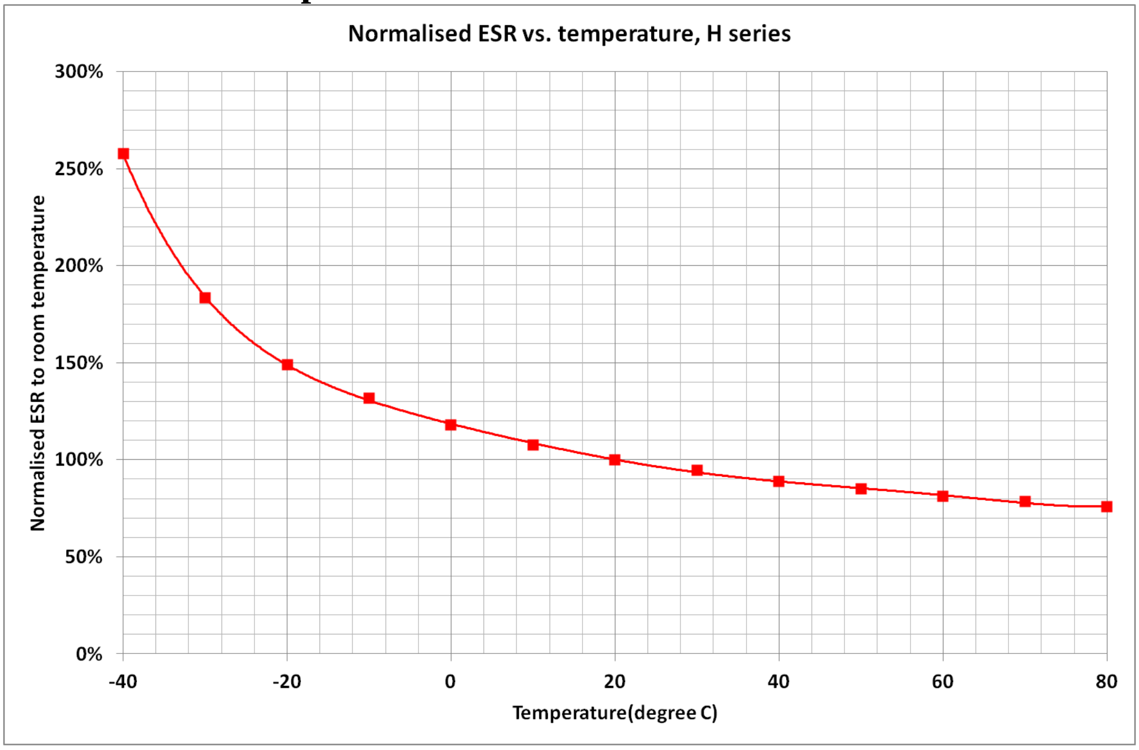

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.1x ESR at room temp, and that ESR at 70ºC is ~0.8 x ESR at room temperature.

Frequency Response

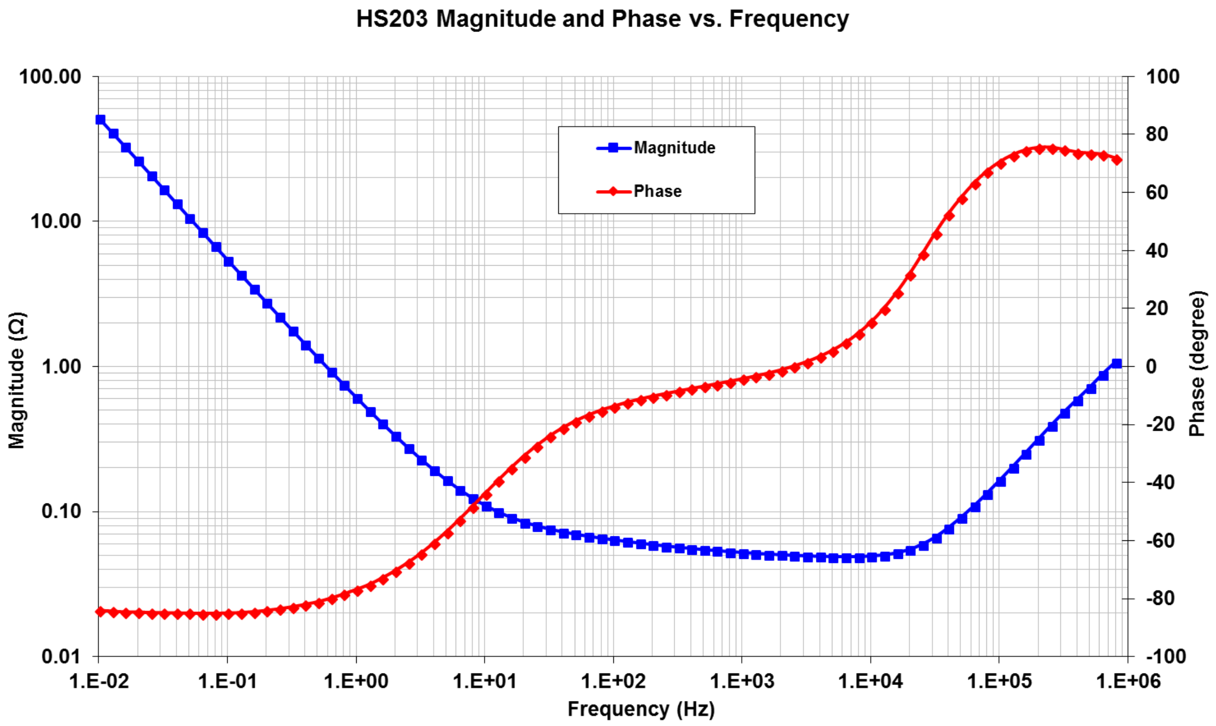

Fig 8: Frequency Response of Impedance (biased at 5.5V with a 50mV test signal)

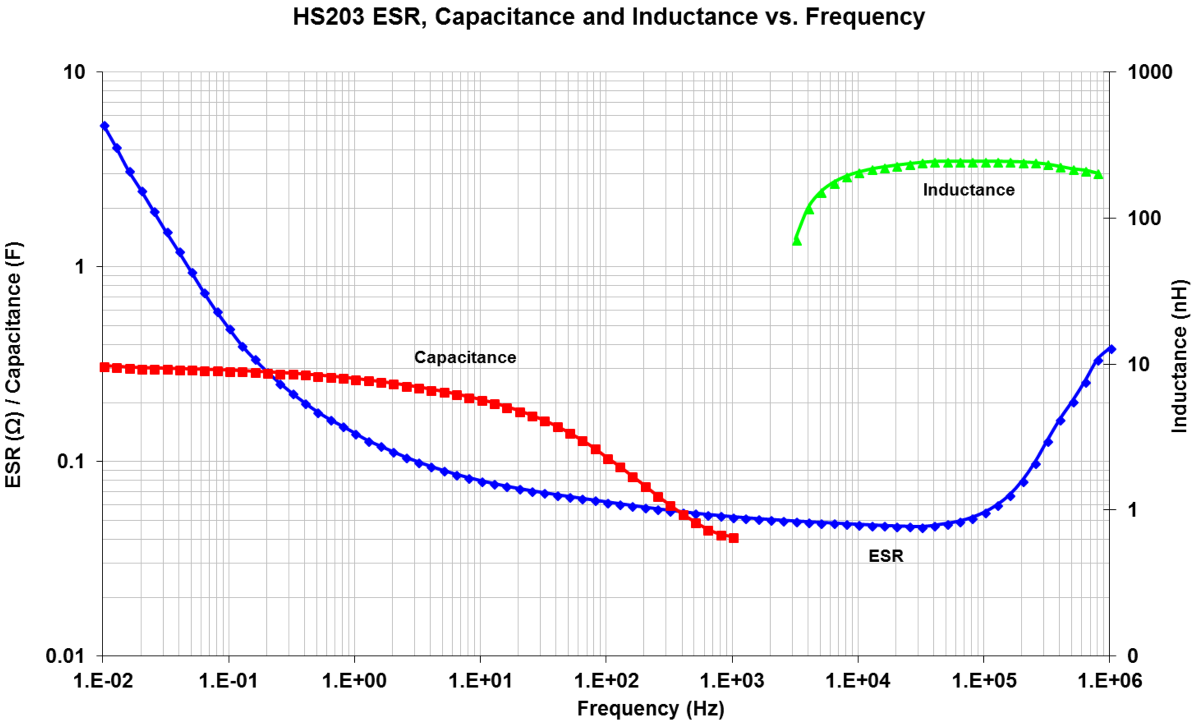

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 9 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

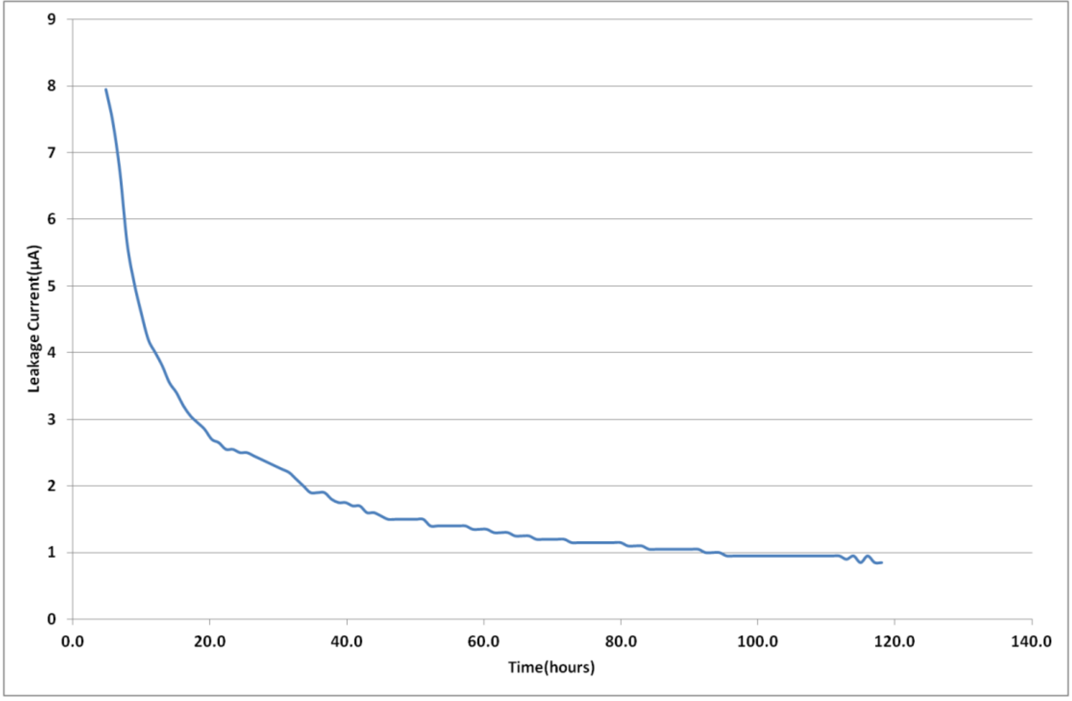

Fig 10: Leakage Current

Fig 10 shows the leakage current for HS103 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1µA at room temperature. At 70°C leakage current will be ~5µA.

Charge Current

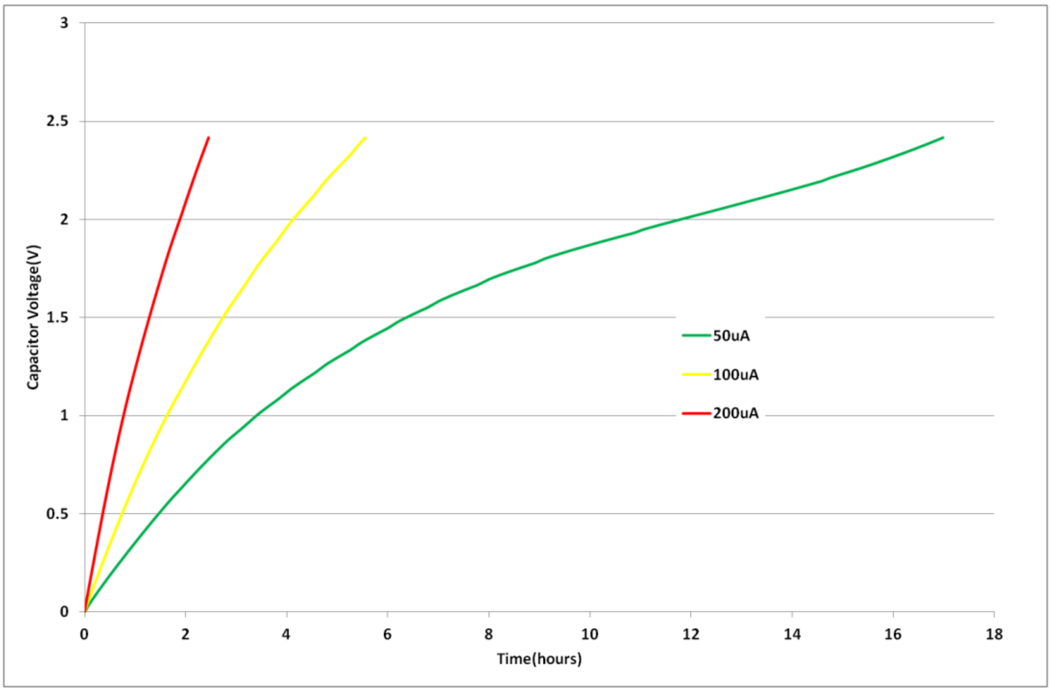

Fig 11: Charging an HS103 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 0.5F x 2.4V / 0.00005A = 6.7hrs to charge a 0.5 F supercapacitor to 2.4V at 50µA, but Fig 11 shows it took 17hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

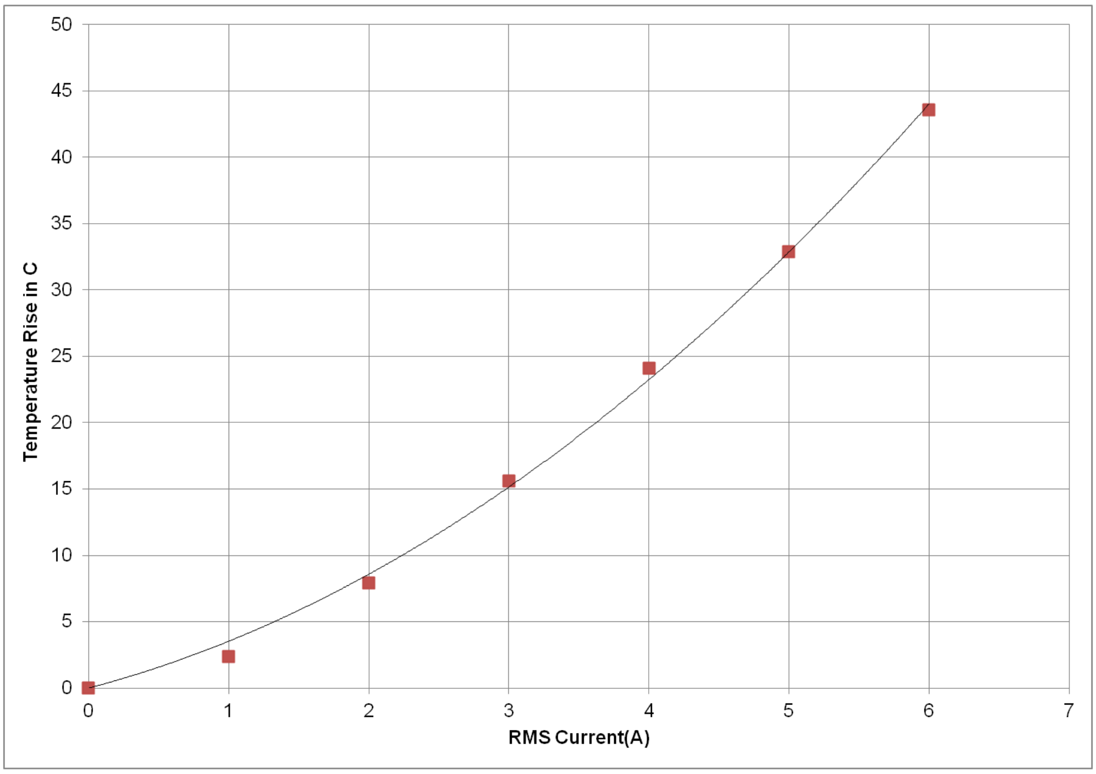

Fig 12: Temperature rise in HS203 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 4.5A, which causes a 30°C temperature increase.

CAP-XX Supercapacitors Product Guide

Refer to the package drawings in the CAP-XX Supercapacitors Product Guide for detailed information of the product's dimensions, PCB landing placements, active areas and electrical connections.

Refer to the CAP-XX Supercapacitors Product Guide for information on endurance and shelf life, transportation and storage, assembly and soldering, safety and RoHS/EREACH certification.

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HS106 / HS206 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HS106 is a single cell supercapacitor. The HS206 is a dual cell supercapacitor with two HS106 cells in series, so HS206 capacitance = Capacitance of HS106/2 and HS206 ESR = 2 x HS106 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HS106		0		2.9	V
		HS206				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HS106		0		2.75	V
		HS206		0		5.5	
Capacitance	C	HS106	DC, 23°C	1040	1300	1560	mF
		HS206		520	650	780	
ESR	ESR	HS106	DC, 23°C		30	36	mΩ
		HS206			55	66	
Leakage Current	I_L		2.75V, 23°C 120hrs		1	2	µA
RMS Current	I_{RMS}		23°C			6	A
Peak Current[1]	I_P		23°C			30	A

[1] Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HS106F	**1.3mm**	No adhesive tape on underside of the supercapacitor	**HS106G**	**1.4mm**	Adhesive tape on underside, release tape removed
HS206F	**2.7mm**		**HS206G**	**2.8mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

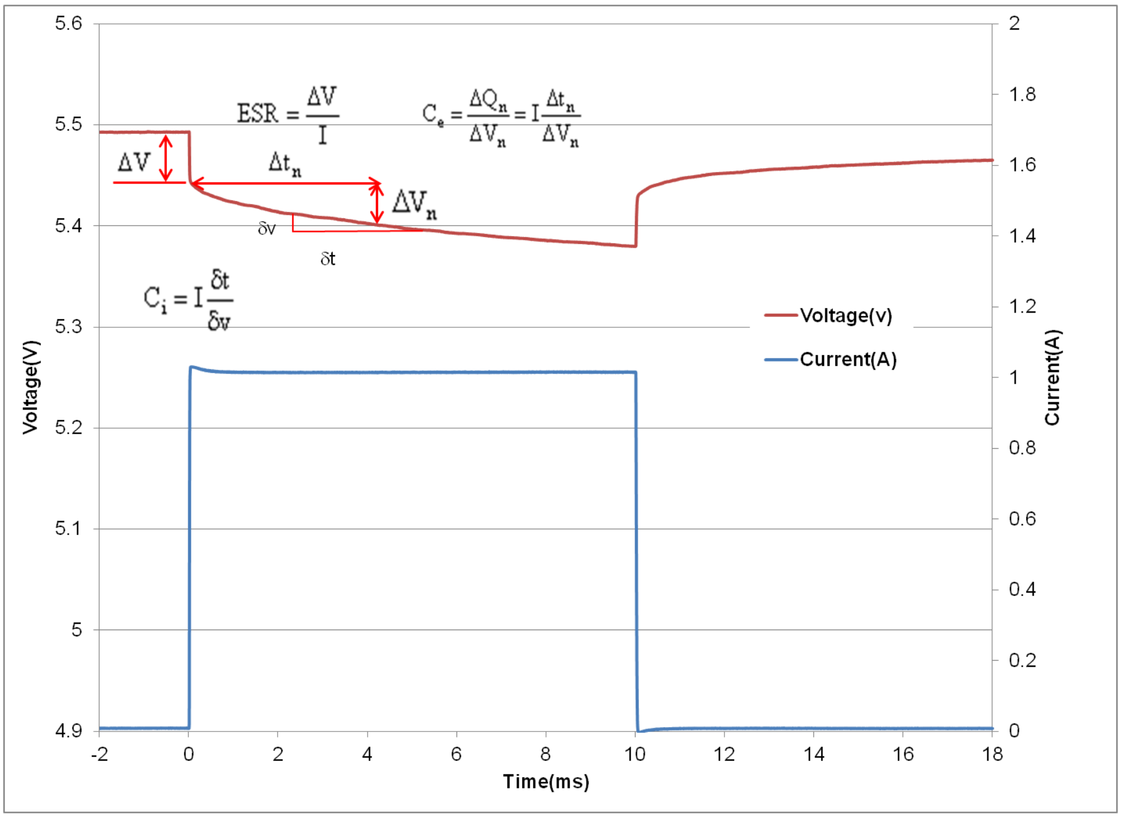

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HS206

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.492V - 5.446V)/1A = 46mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I$ x $\Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.446 V – 5.413V) = 33mV. Therefore Ce(2ms) = 1A x 2ms/33mV = 60.6mF. After 10ms, the voltage drop = 5.446 V – 5.379V = 67mV. Therefore Ce(10ms) = 1 A x 10ms/67mV = 149mF. The DC capacitance of an HS206 = 0.65 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

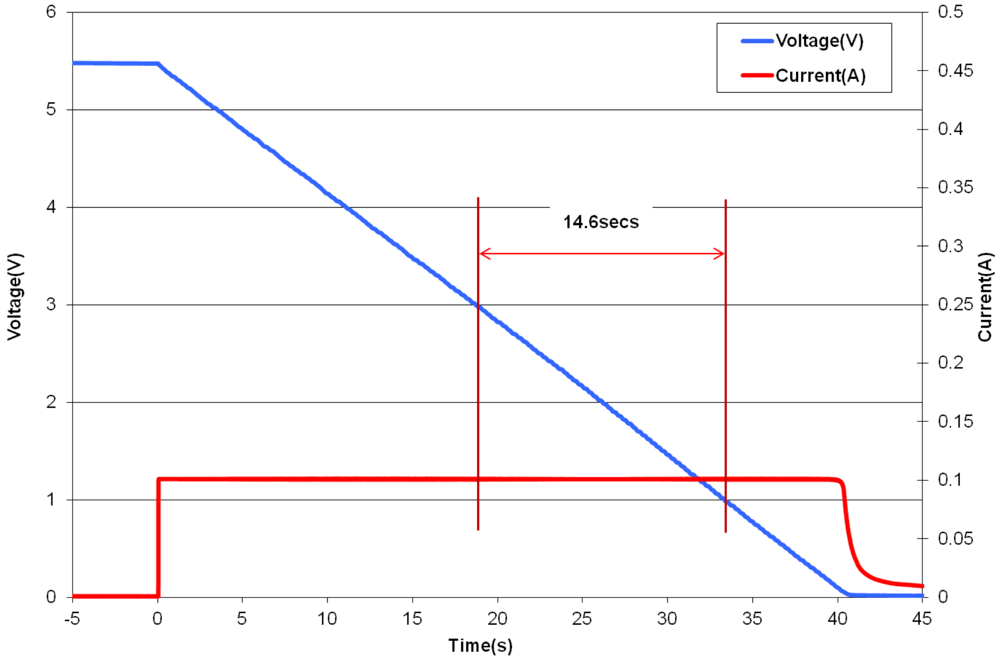

Fig 2: Measurement of DC Capacitance for an HS206

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 14.6s /2V = 730mF, which is well within the 650mF +/- 20% tolerance for an HS206 cell.

Measurement of ESR

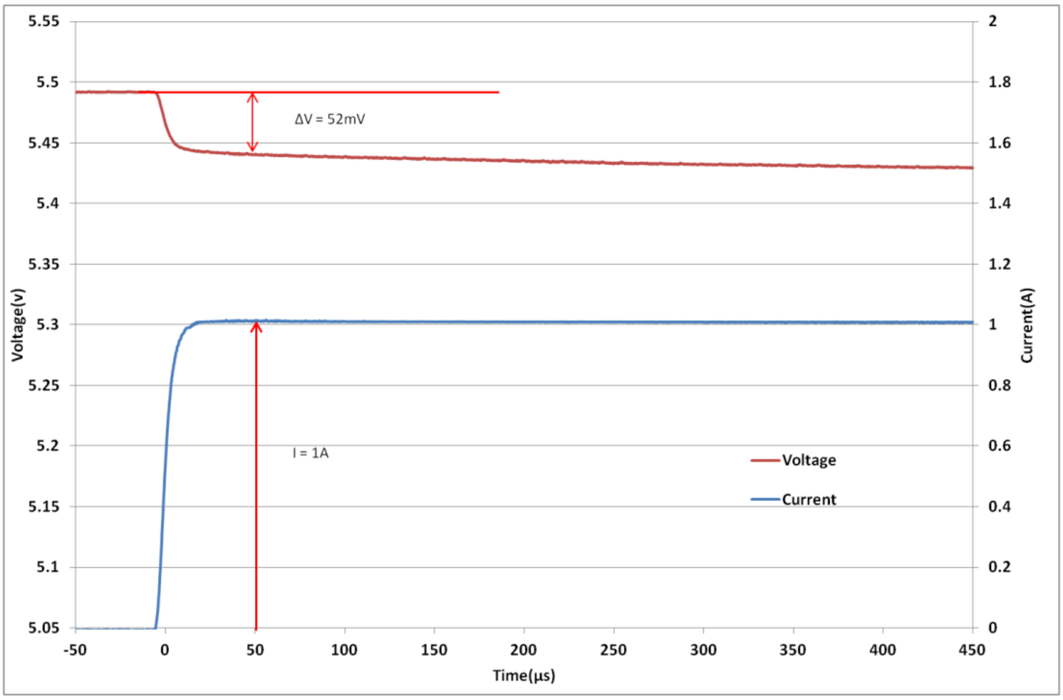

Fig 3: Measurement of ESR for an HS206

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 52mV/1A = 52mΩ.

Effective Capacitance

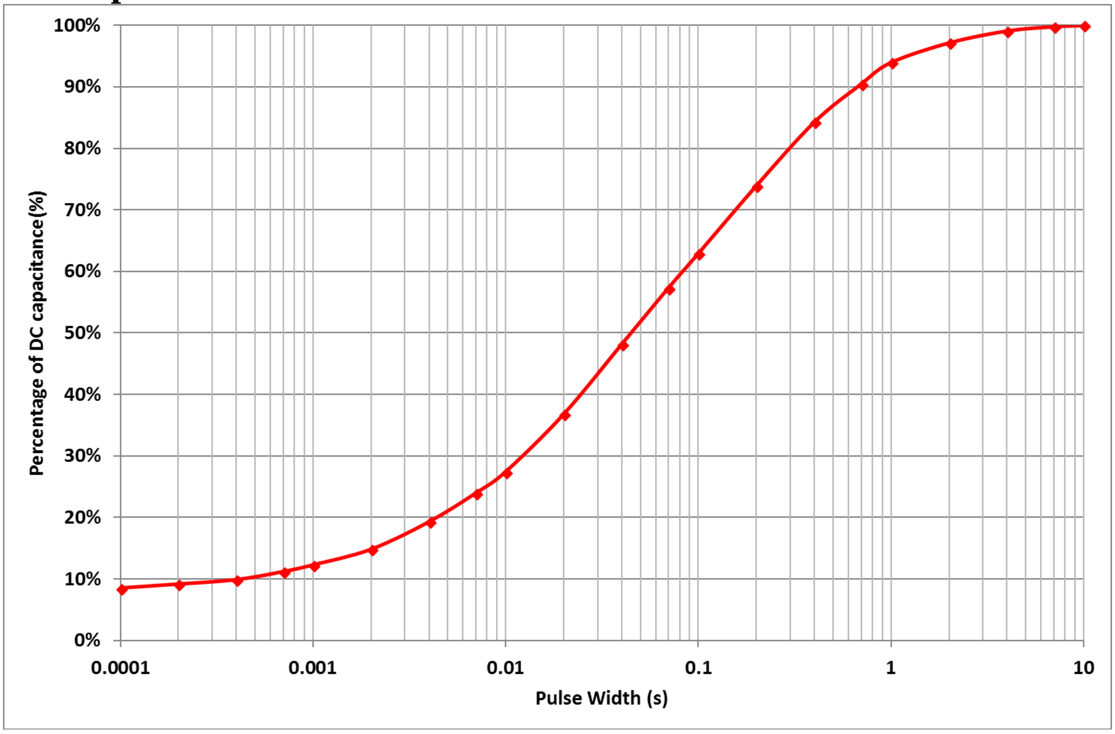

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HS106, HS206 @ 23°C. This shows that for a 1ms PW, you will measure 12% of DC capacitance or 156mF for an HS106 or 78mF for an HS206. At 10ms you will measure 27% of the DC capacitance, and at 100ms you will measure 63% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10ms, then you would use the Ceff(10ms) = 27% of DC capacitance = 176mF for an HS206, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 55mΩ + 1A x 10ms / 176mF = 112mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

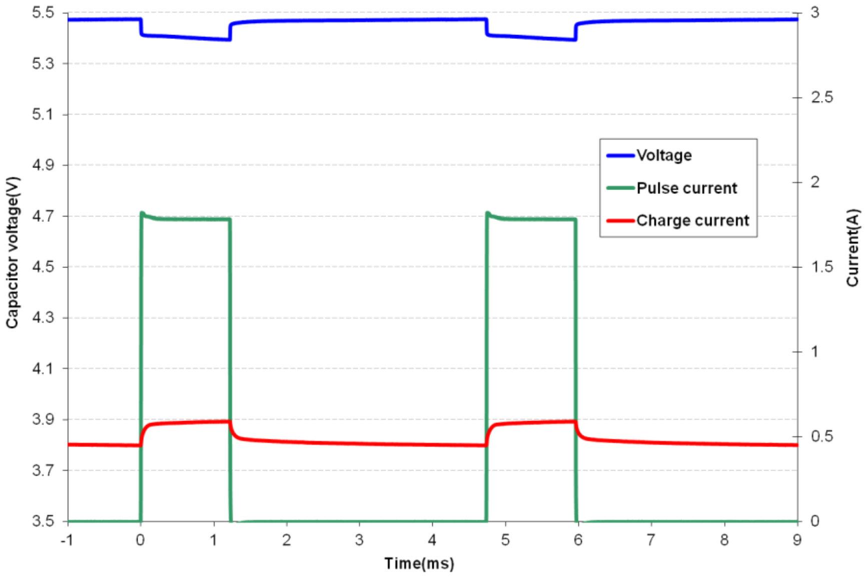

Fig 5 shows that the HS206 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 65mF coupled with the low ESR supports this pulse train with only ~80mV droop in the supply rail.

Fig 5: HS206 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

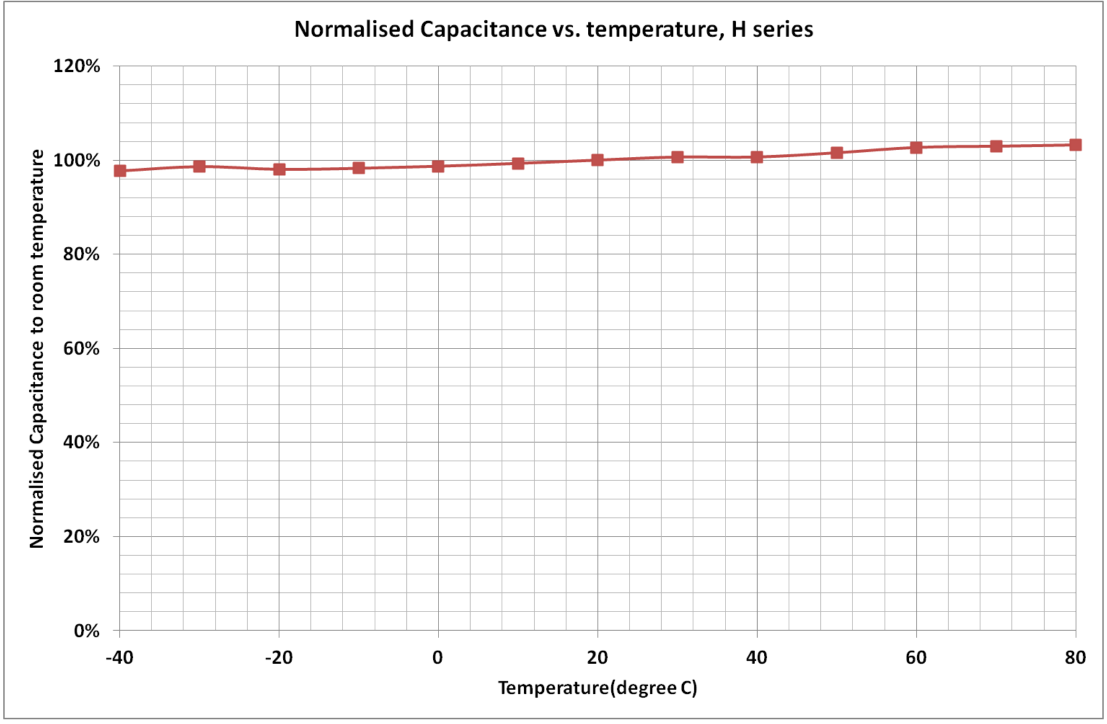

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

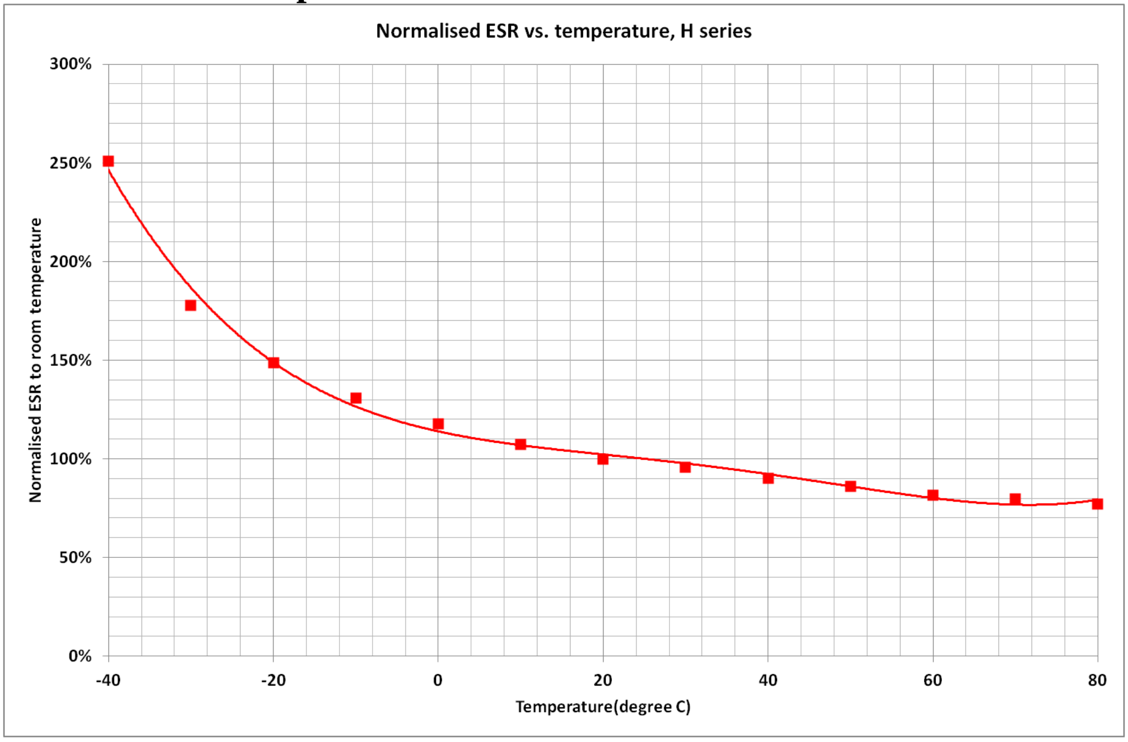

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.5 x ESR at room temp, and that ESR at 70°C is ~0.8 x ESR at room temperature.

Frequency Response

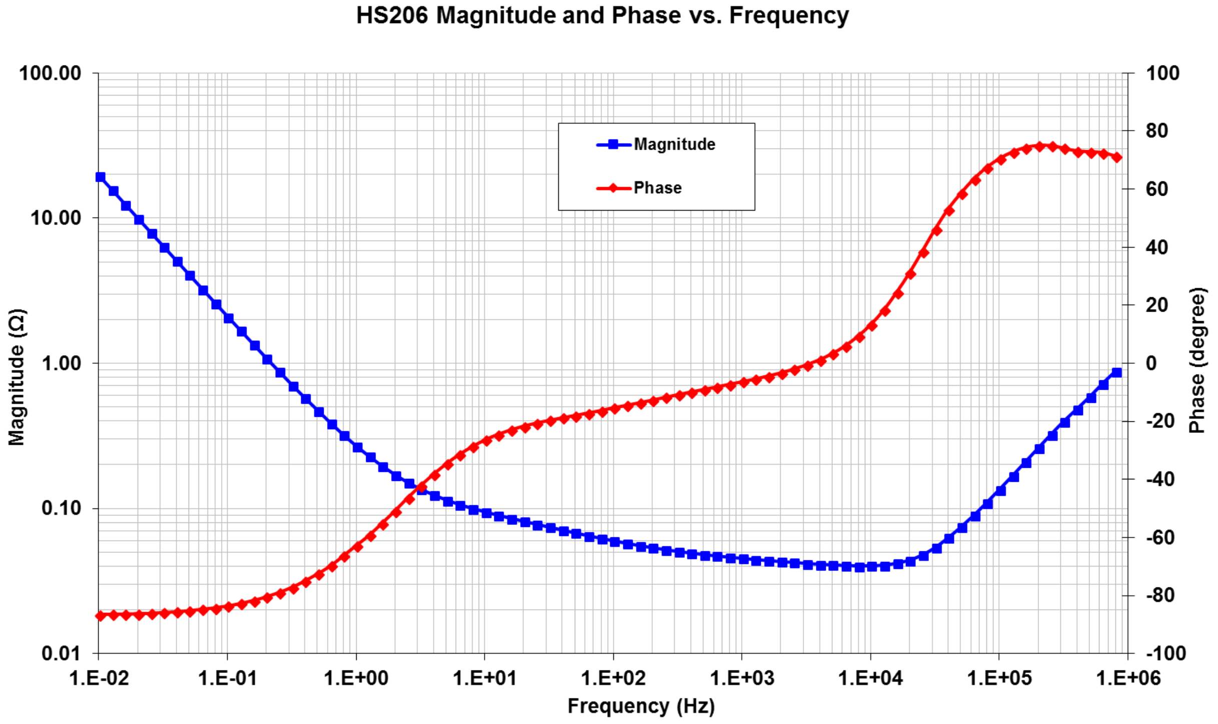

Fig 8: Frequency Response of Impedance (biased at 5.5V with a 50mV test signal)

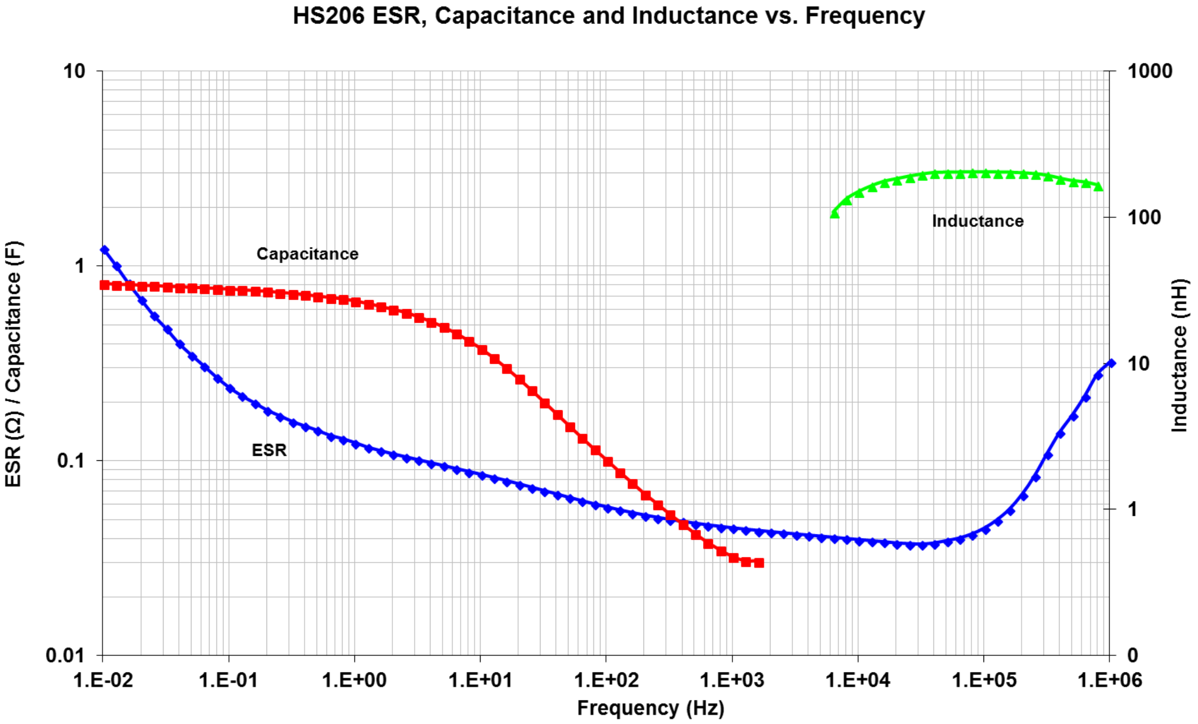

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 2.5 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

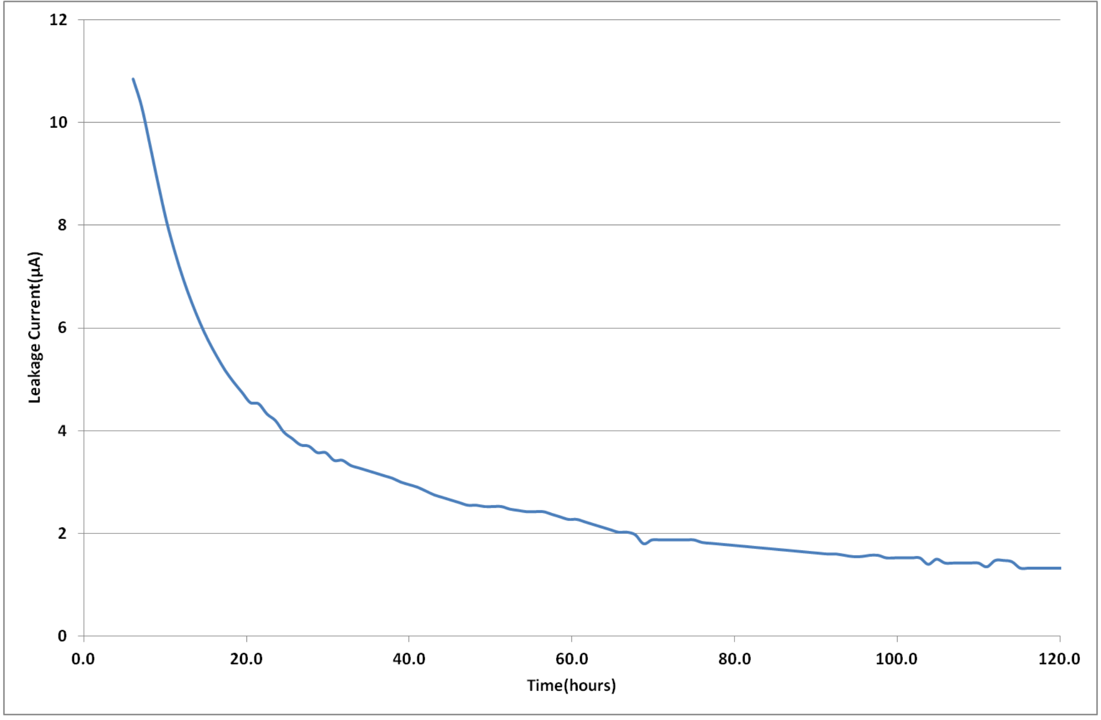

Fig 10: Leakage Current

Fig 10 shows the leakage current for HS106 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1.5µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

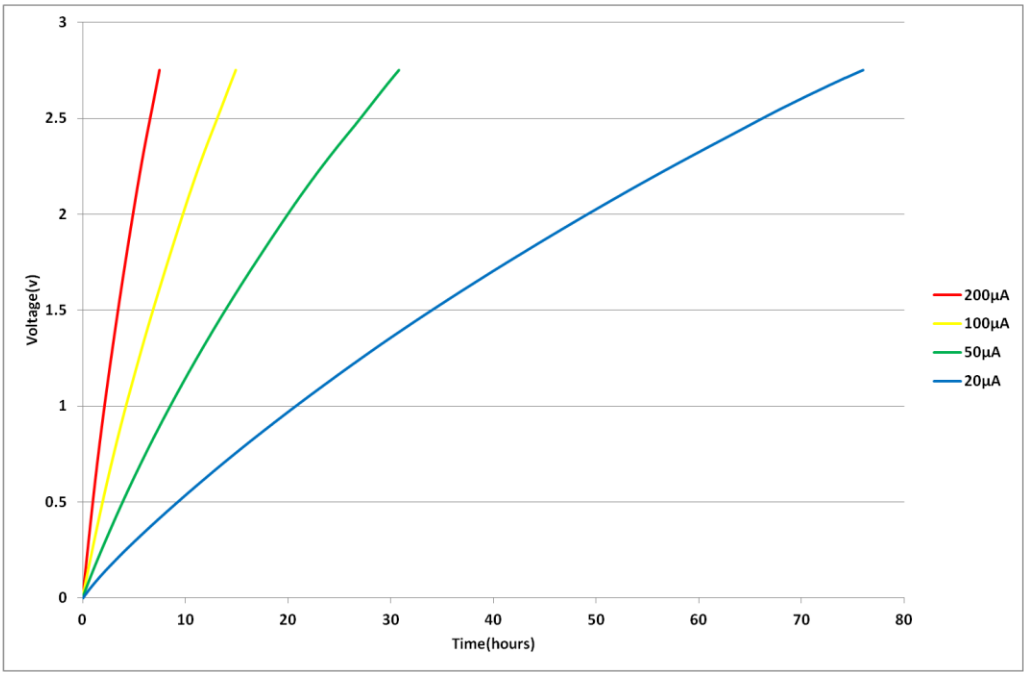

Fig 11: Charging an HS106 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 1.3 F x 2.7V / 0.00002A = 43.3hrs to charge a 1.3 F supercapacitor to 2.7V at 20µA, but Fig 11 shows it took 75hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

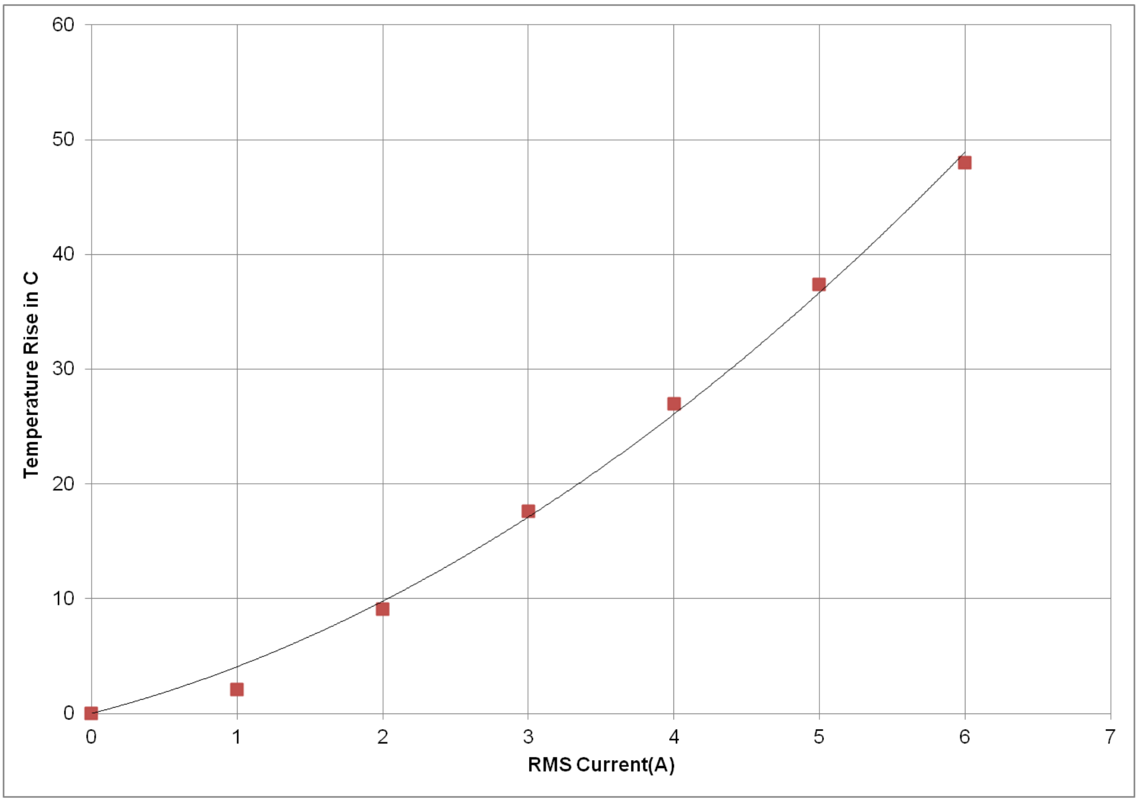

Fig 12: Temperature rise in HS206 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 4.3A, which causes a 30°C temperature increase.

CAP-XX Supercapacitors Product Guide

Refer to the package drawings in the CAP-XX Supercapacitors Product Guide for detailed information of the product’s dimensions, PCB landing placements, active areas and electrical connections.

Refer to the CAP-XX Supercapacitors Product Guide for information on endurance and shelf life, transportation and storage, assembly and soldering, safety and RoHS/EREACH certification.

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HS108 / HS208 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HS108 is a single cell supercapacitor. The HS208 is a dual cell supercapacitor with two HS108 cells in series, so HS208 capacitance = Capacitance of HS108/2 and HS208 ESR = 2 x HS108 ESR.

Table 1: Absolute Maximum Ratings

Parameter	**Name**		**Conditions**	**Min**	**Typical**	**Max**	**Units**
Terminal Voltage	Vpeak	HS108		0		2.9	V
		HS208				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	**Name**		**Conditions**	**Min**	**Typical**	**Max**	**Units**
Terminal Voltage	Vn	HS108		0		2.75	V
		HS208		0		5.5	
Capacitance	C	HS108	DC, 23°C	1440	1800	2160	mF
		HS208		720	900	1080	
ESR	ESR	HS108	DC, 23°C		25	30	mΩ
		HS208			45	54	
Leakage Current	I_L		2.75V, 23°C 120hrs		2	4	µA
RMS Current	I_{RMS}		23°C			5	A
Peak Current[1]	I_P		23°C			30	A

[1] Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HS108F	**1.7mm**	No adhesive tape on underside of the supercapacitor	**HS108G**	**1.8mm**	Adhesive tape on underside, release tape removed
HS208F	**3.4mm**		**HS208G**	**3.5mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 sec.

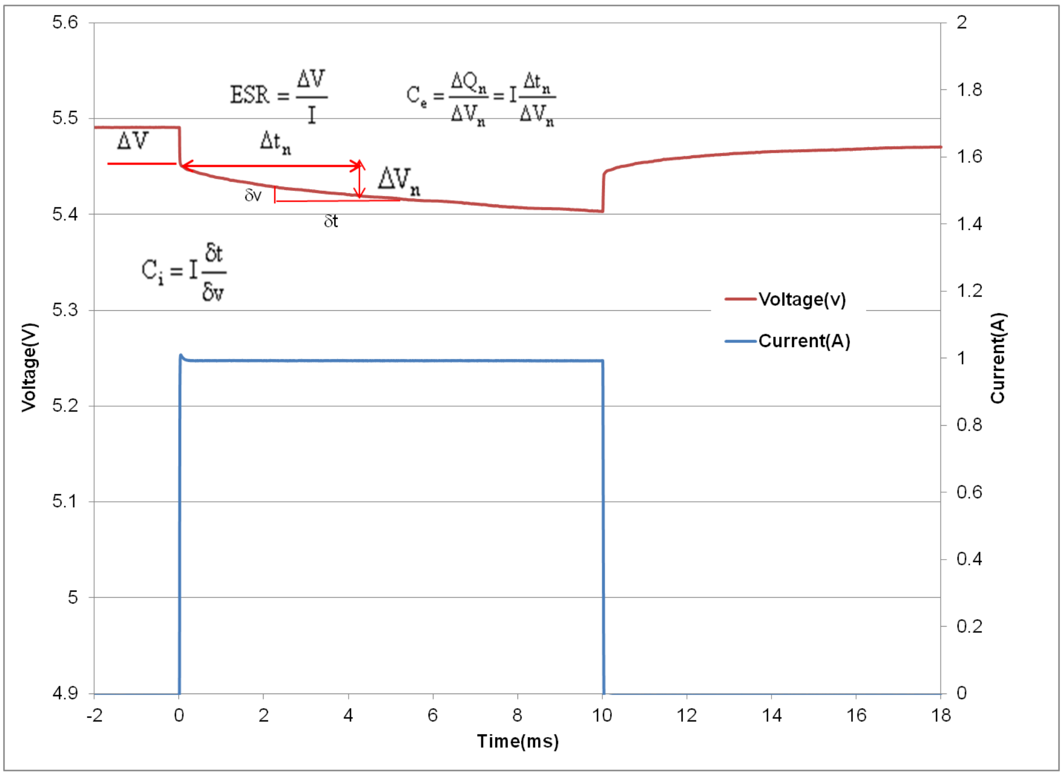

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HS208

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.49V - 5.457V)/1A = 33mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, Ce(Δt_n) is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current Ce(Δt_n) = I x $\Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.457 V – 5.429V) = 28mV. Therefore Ce(2ms) = 1A x 2ms/28mV = 71mF. After 10ms, the voltage drop = 5.457 V – 5.403V = 54mV. Therefore Ce(10ms) = 1 A x 10ms/54mV = 185mF. The DC capacitance of an HS208 = 0.9 F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

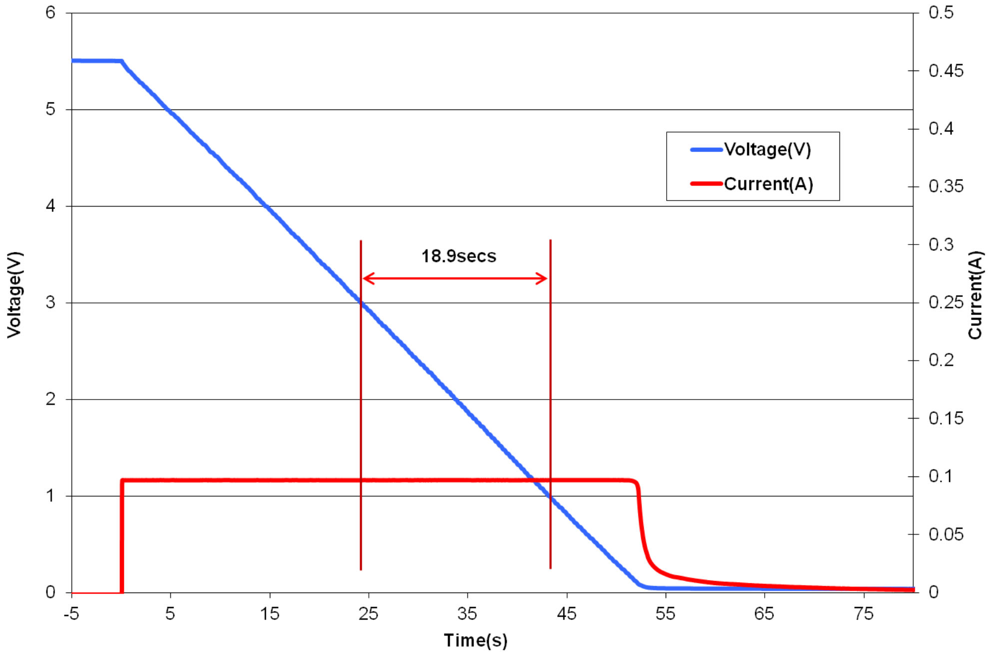

Fig 2: Measurement of DC Capacitance for an HS208

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 18.9s /2V = 945mF, which is well within the 0.9F +/- 20% tolerance for an HS208 cell.

Measurement of ESR

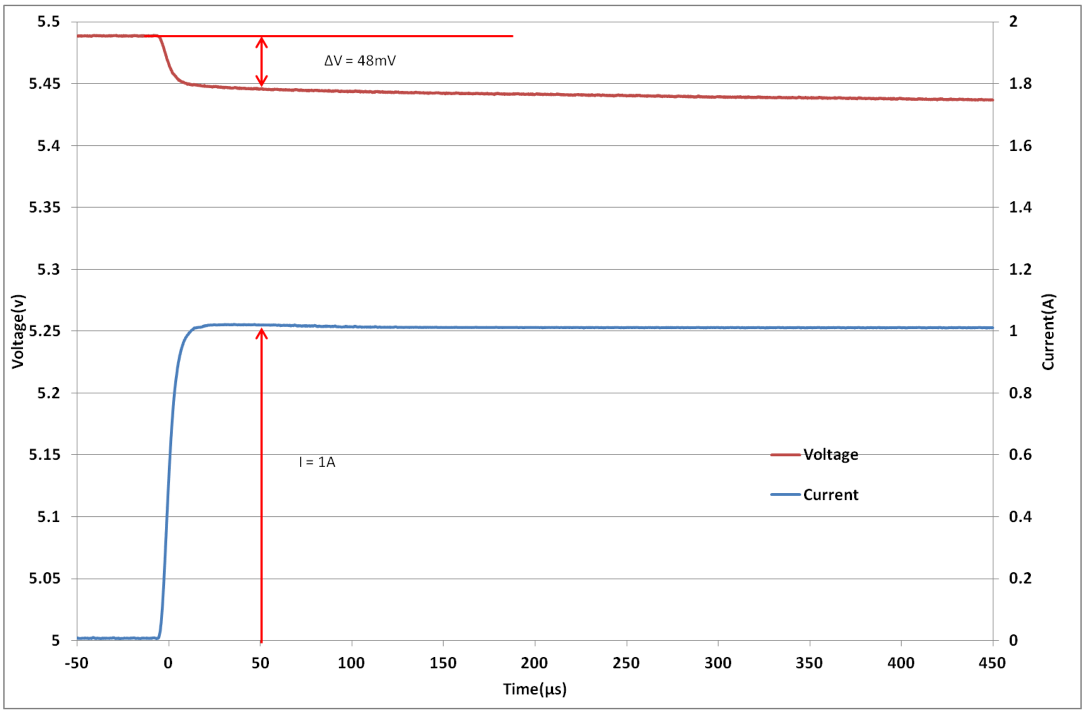

Fig 3: Measurement of ESR for an HS208

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 48mV/1.A = 48mΩ.

Effective Capacitance

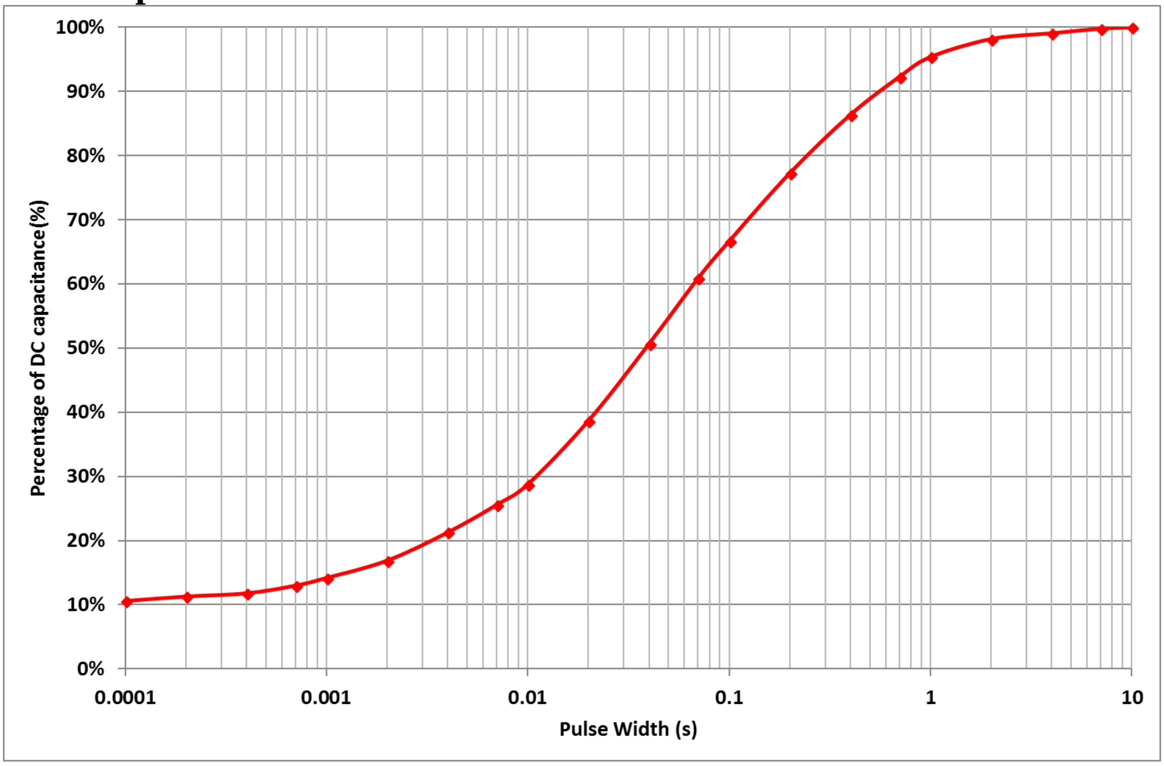

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HS108, HS208 @ 23°C. This shows that for a 1mS PW, you will measure 14% of DC capacitance or 252mF for an HS108 or 126mF for an HS208. At 10ms you will measure 29% of the DC capacitance, and at 100ms you will measure 67% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10ms, then you would use the Ceff(10ms) = 29% of DC capacitance = 261mF for an HS208, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 45mΩ + 1A x 10ms / 261mF = 83.3mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

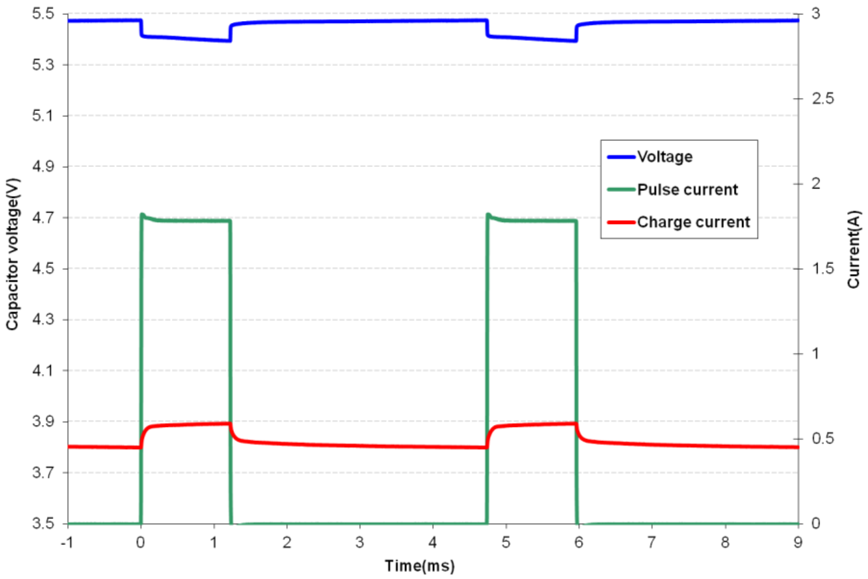

Fig 5 shows that the HS208 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacacitor would not support a 1ms pulse, but the Ceff of 72mF coupled with the low ESR supports this pulse train with only ~80mV droop in the supply rail.

Fig 5: HS208 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

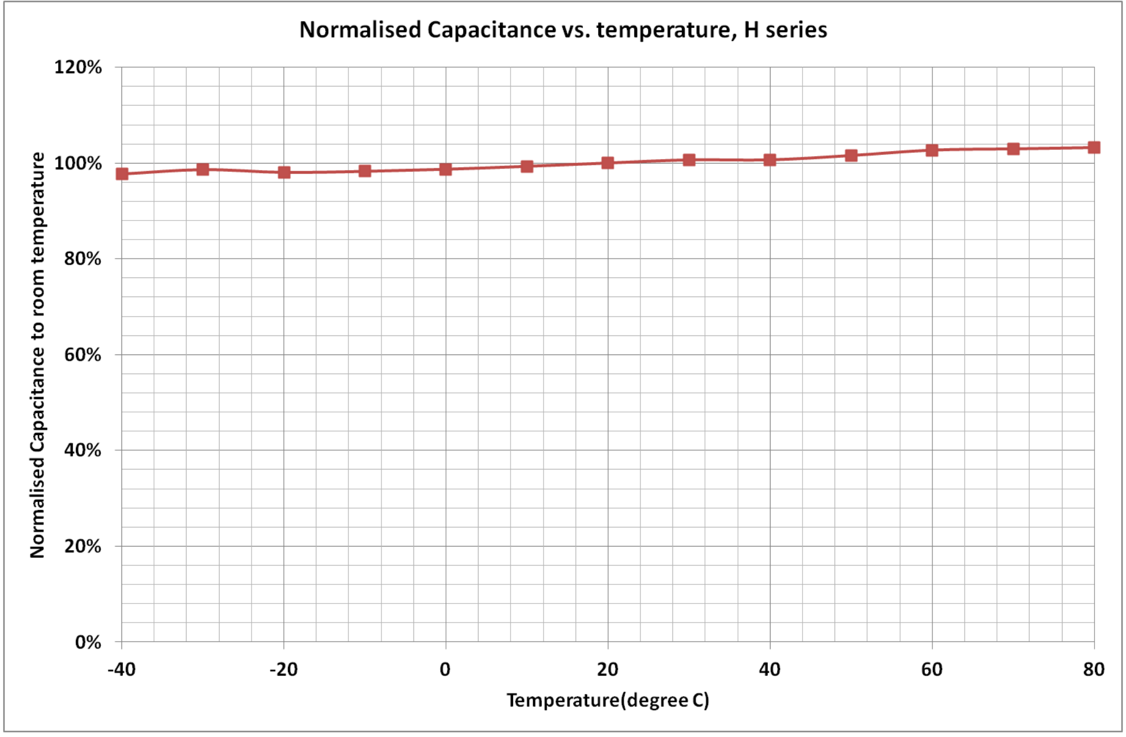

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

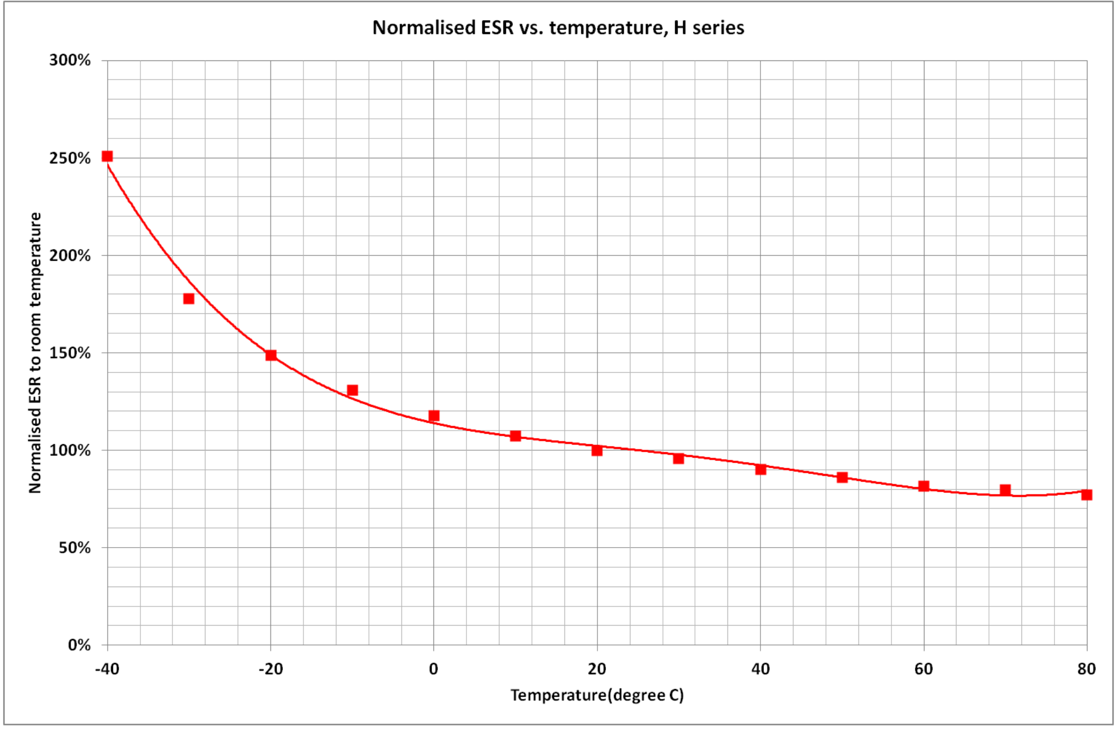

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~2.5 x ESR at room temp, and that ESR at 70ºC is ~0.8 x ESR at room temperature.

Frequency Response

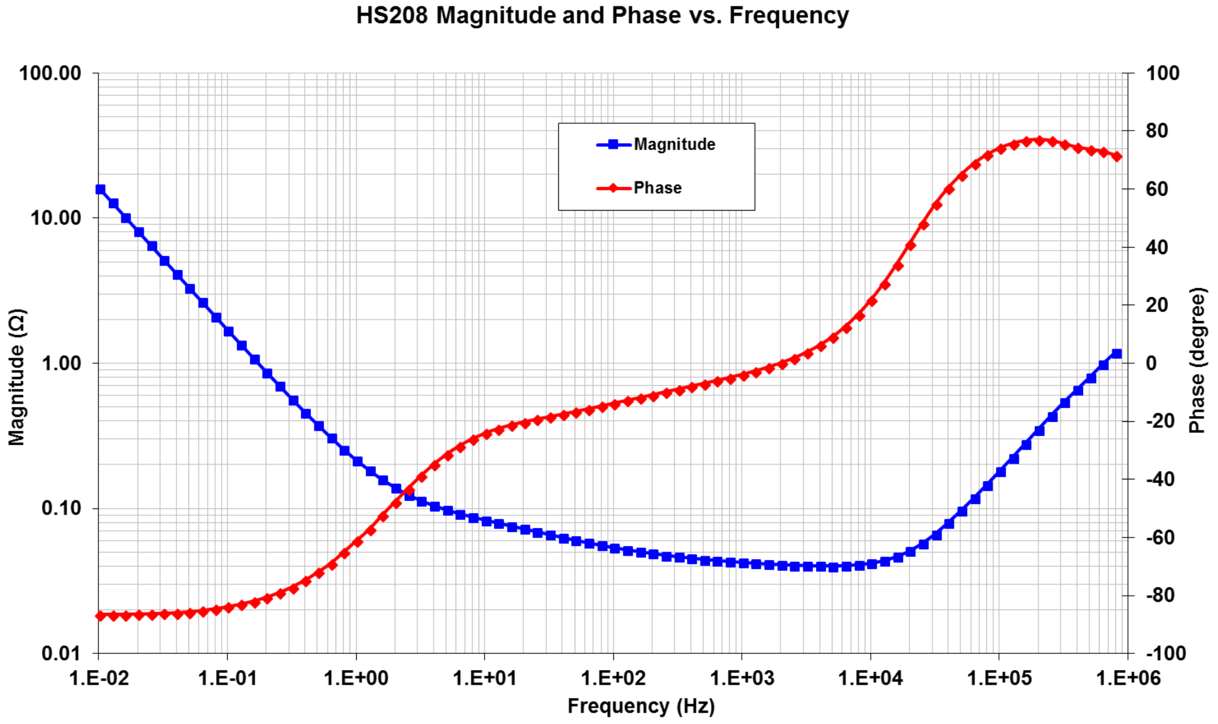

Fig 8: Frequency Response of Impedance (biased at 5.5V with a 50mV test signal)

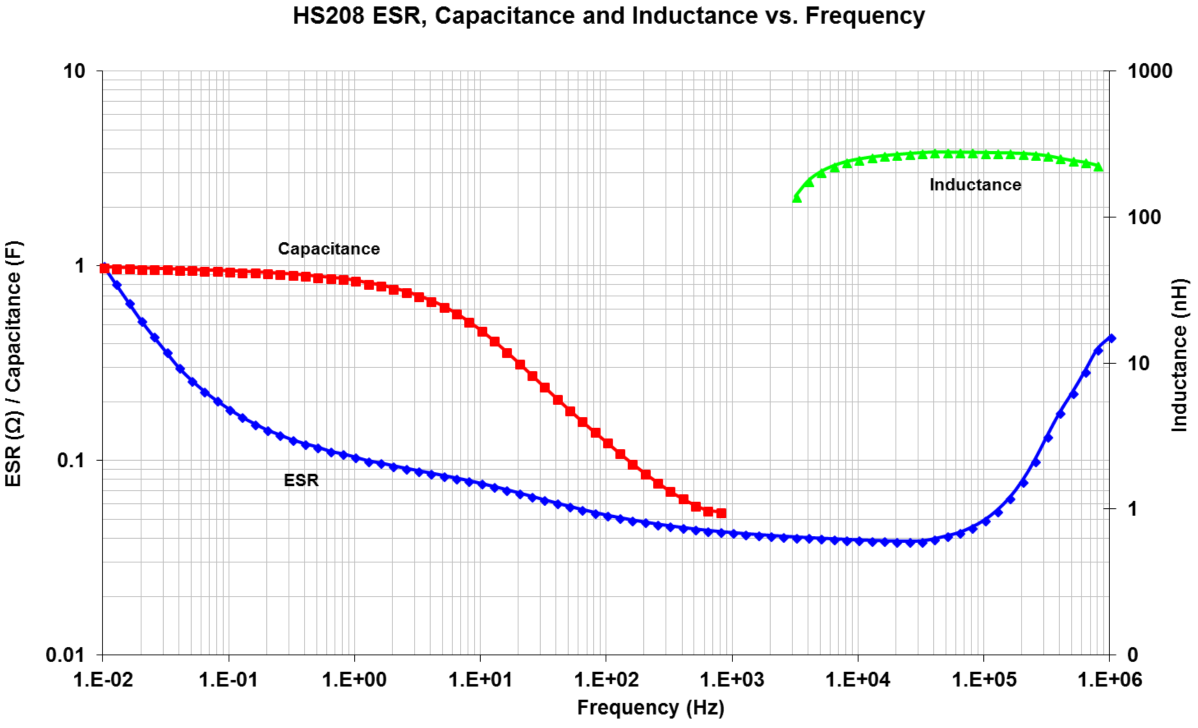

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 2 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

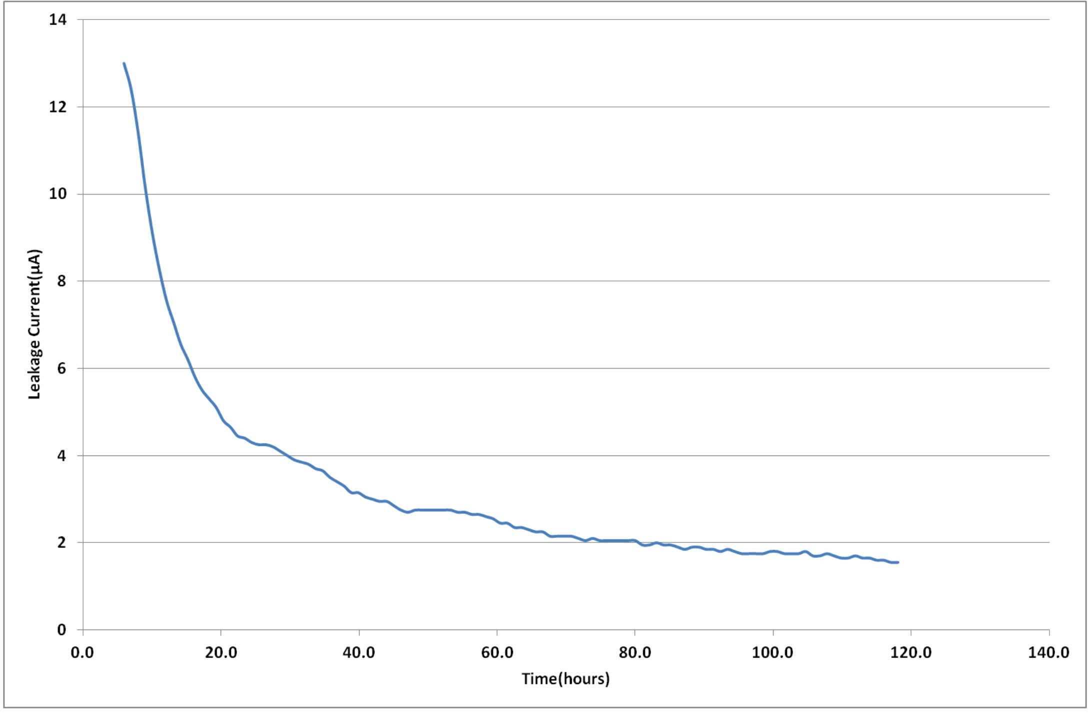

Fig 10: Leakage Current

Fig 10 shows the leakage current for HS108 at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 1.5µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

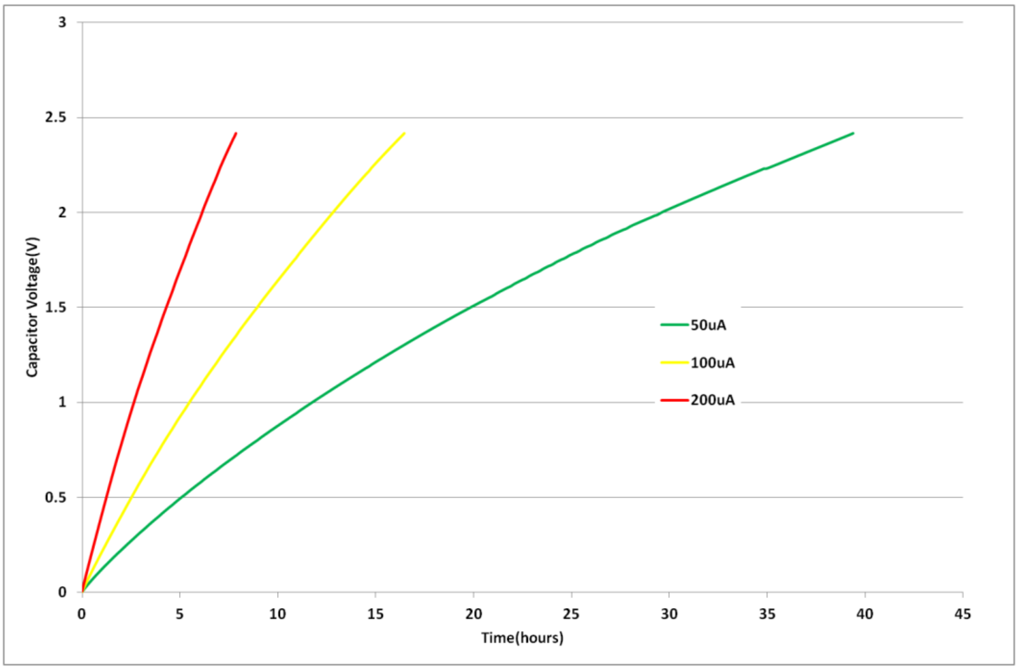

Fig 11: Charging an HS108 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 1.8 F x 2.4V / 0.00005A = 24hrs to charge a 1.8 F supercapacitor to 2.4V at 50µA, but Fig 11 shows it took 40hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

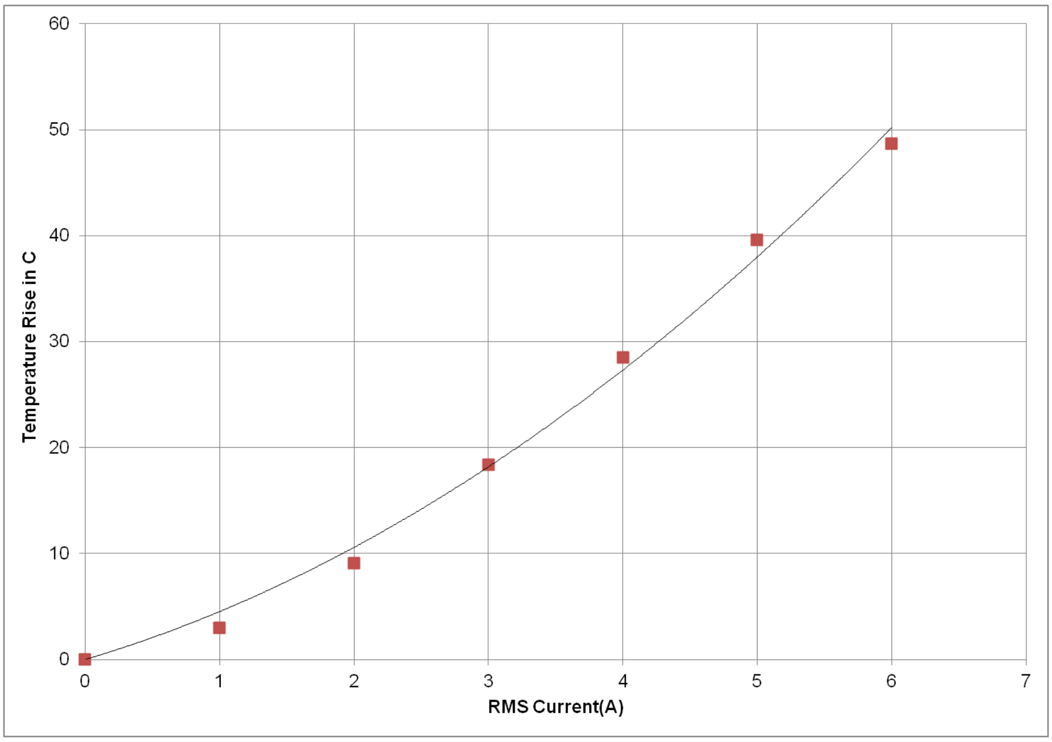

Fig 12: Temperature rise in HS208 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 4A, which causes a 30°C temperature increase.

CAP-XX Supercapacitors Product Guide

Refer to the package drawings in the CAP-XX Supercapacitors Product Guide for detailed information of the product’s dimensions, PCB landing placements, active areas and electrical connections.

Refer to the CAP-XX Supercapacitors Product Guide for information on endurance and shelf life, transportation and storage, assembly and soldering, safety and RoHS/EREACH certification.

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HS130 / HS230 SUPERCAPACITOR

Datasheet Rev 4.3, July 2018

This Datasheet should be read in conjunction with the CAP-XX Supercapacitors Product Guide which contains information common to our product lines.

Electrical Specifications

The HS130 is a single cell supercapacitor. The HS230 is a dual cell supercapacitor with two HS130 cells in series, so HS230 capacitance = Capacitance of HS130/2 and HS230 ESR = 2 x HS130 ESR.

Table 1: Absolute Maximum Ratings

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vpeak	HS130		0		2.9	V
		HS230				5.8	
Temperature	Tmax			-40		+85	°C

Table 2: Electrical Characteristics

Parameter	Name		Conditions	Min	Typical	Max	Units
Terminal Voltage	Vn	HS130		0		2.75	V
		HS230		0		5.5	
Capacitance	C	HS130	DC, 23°C	1920	2400	2880	mF
		HS230		960	1200	1440	
ESR	ESR	HS130	DC, 23°C		25	30	mΩ
		HS230			45	54	
Leakage Current	I_L		2.75V, 23°C 120hrs		3	5	µA
RMS Current	I_{RMS}		23°C			6	A
Peak Current[1]	I_P		23°C			30	A

[1] Non-repetitive current, single pulse to discharge fully charged supercapacitor.

Table 3: Thickness

HS130F	**1.9mm**	No adhesive tape on underside of the supercapacitor	**HS130G**	**1.9mm**	Adhesive tape on underside, release tape removed
HS230F	**3.9mm**		**HS230G**	**4.0mm**	

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, I =1A for duration 0.01 secs.

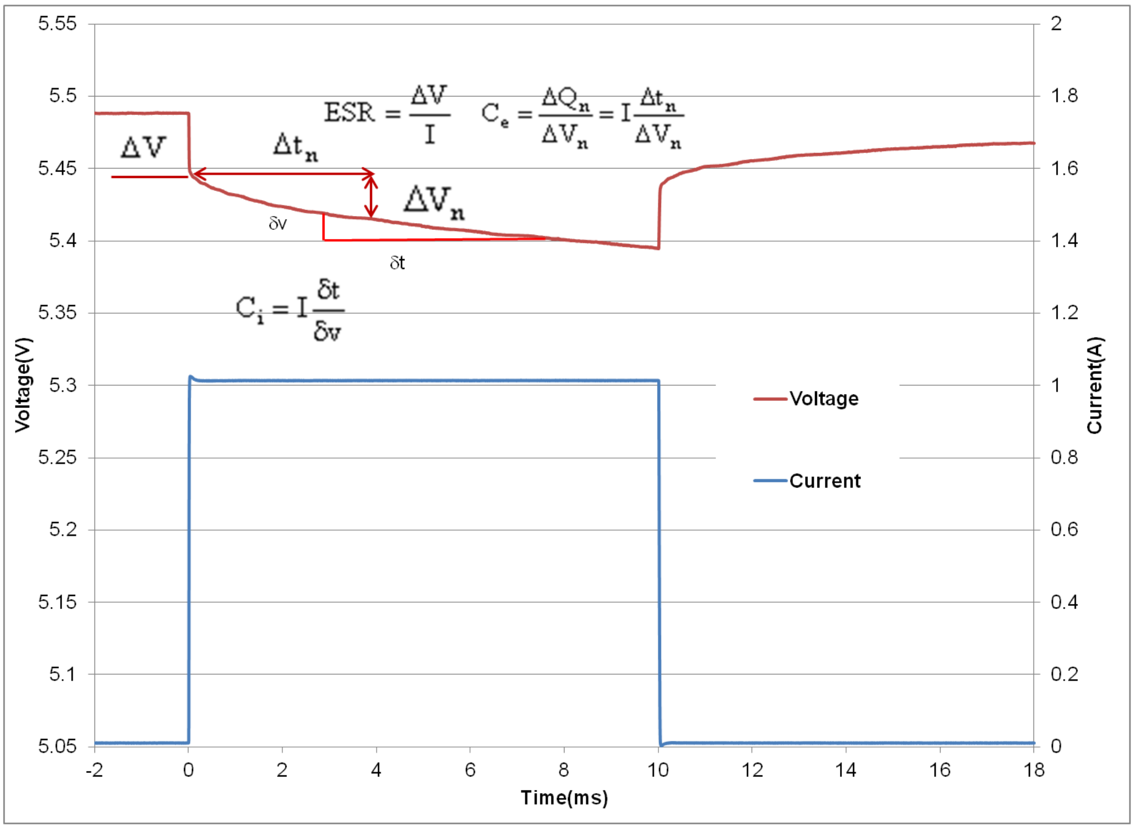

Figure 1: Effective capacitance, instantaneous capacitance and ESR for an HS230

The ESR is found by dividing the instantaneous voltage step (ΔV) by I. In this example = (5.488 V-5.452V)/1.01A = 36mΩ.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I.

The effective capacitance for a pulse of duration Δt_n, $Ce(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $Ce(\Delta t_n) = I \times \Delta t_n/\Delta V_n$. Ce increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop V_{2ms} = (5.452 V – 5.424V) = 28mV. Therefore Ce(2ms) = 1.01A x 2ms/28mV =71mF. After 10ms, the voltage drop = 5.452V – 5.395V = 57mV. Therefore Ce(10ms) = 1.01A x 10ms/57mV = 175mF. The DC capacitance of an HS230 = 1.2F. Note that ΔV, or IR drop, is not included because very little charge is removed from the capacitor during this time. Ce shows the time response of the capacitor and it is useful for predicting circuit behavior in pulsed applications.

Measurement of DC Capacitance

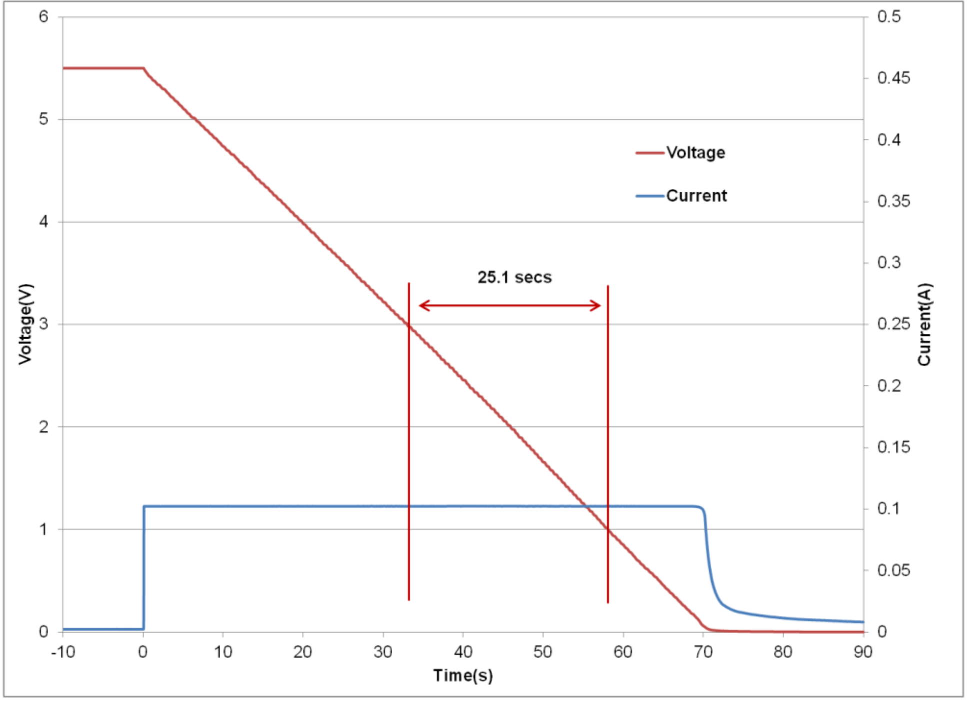

Fig 2: Measurement of DC Capacitance for an HS230

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 1.5V to 0.5V for a single cell, or from 3V to 1V for a dual cell supercapacitor. In this case, C = 0.1A x 25.1 s /2V = 1.255F, which is well within the 1.2F +/- 20% tolerance for an HS230 cell.

Measurement of ESR

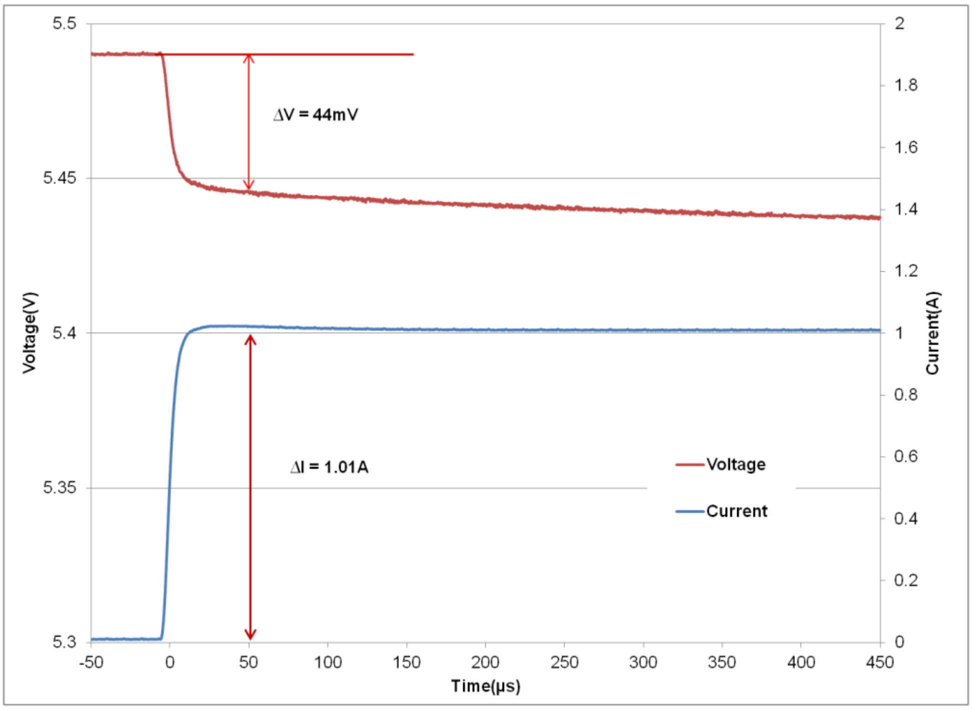

Fig 3: Measurement of ESR for an HS230

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50µs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as 44mV/1.01A = 43.6mΩ.

Effective Capacitance

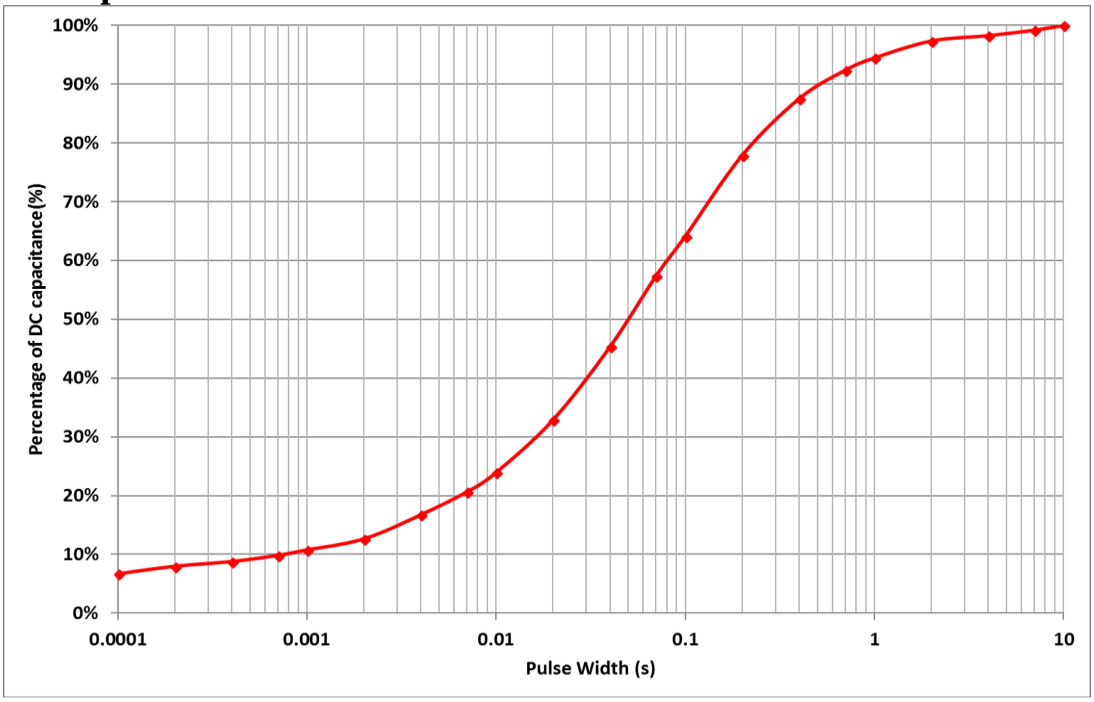

Figure 4: Effective Capacitance

Fig 4 shows the effective capacitance for the HS130, HS230 @ 23°C. This shows that for a 1ms PW, you will measure 11% of DC capacitance or 264mF for an HS130 or 132mF for an HS230. At 10ms you will measure 24% of the DC capacitance, and at 100ms you will measure 64% of DC capacitance. Ceffective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10ms, then you would use the Ceff(10ms) = 24% of DC capacitance = 288mF for an HS230, so Vdrop = 1A x ESR + 1A x duration/C = 1A x 45mΩ + 1A x 10ms / 288mF = 80mV. The next section on pulse response shows how the effective capacitance is sufficient for even short pulse widths.

Pulse Response

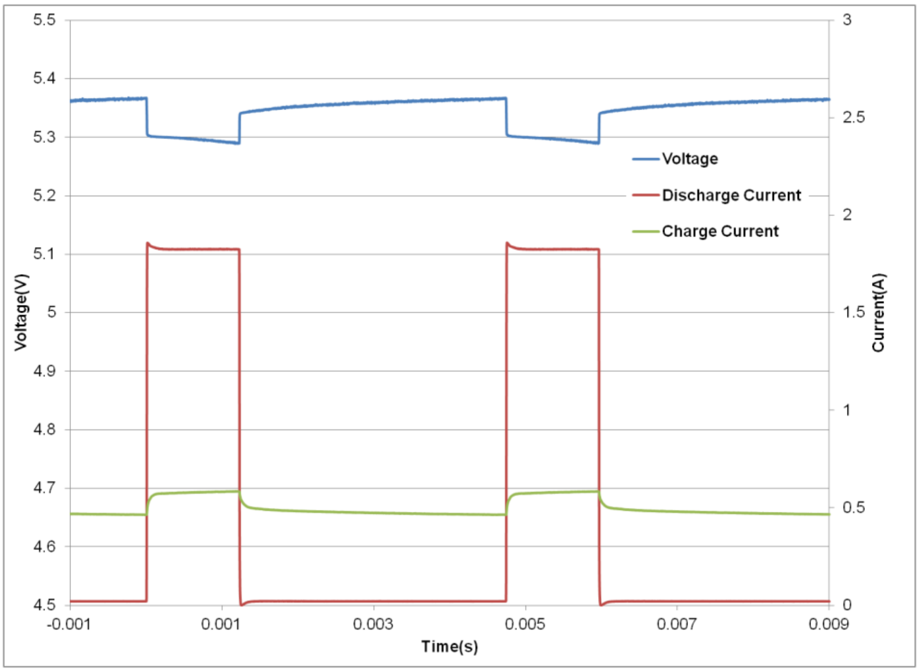

Fig 5 shows that the HS230 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacitor would not support a 1ms pulse, but the Ceff of 108mF coupled with the low ESR supports this pulse train with only ~74mV droop in the supply rail.

Fig 5: HS230 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

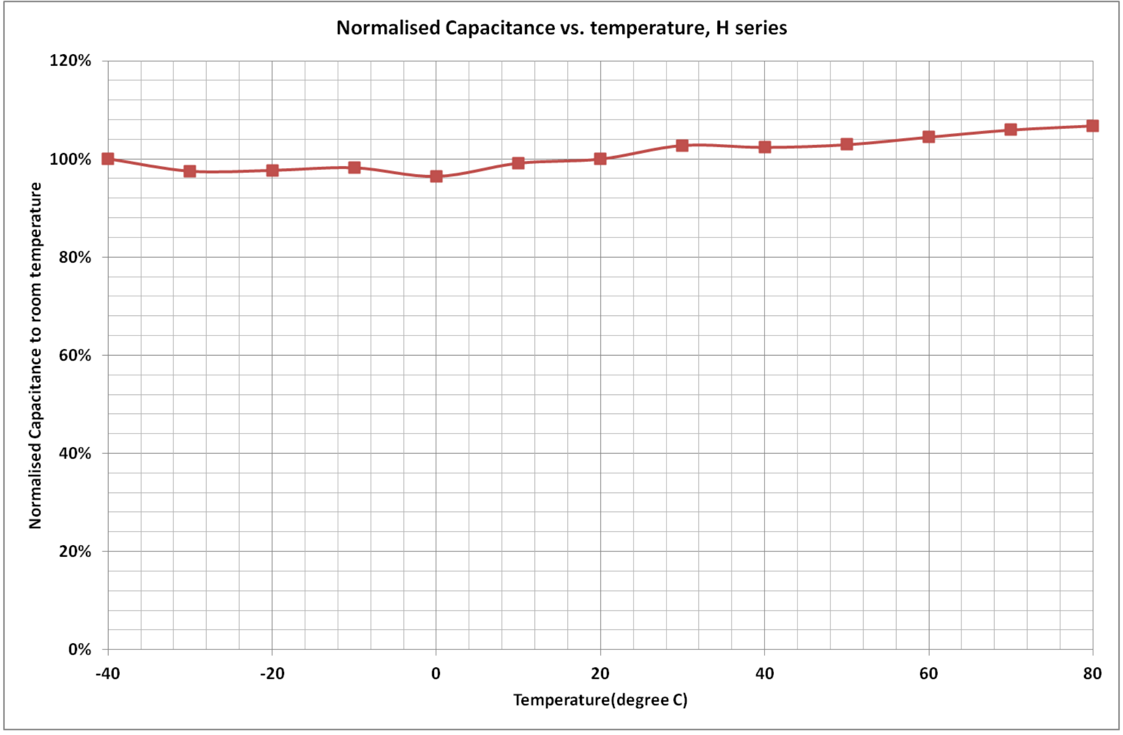

Figure 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature.

ESR variation with temperature

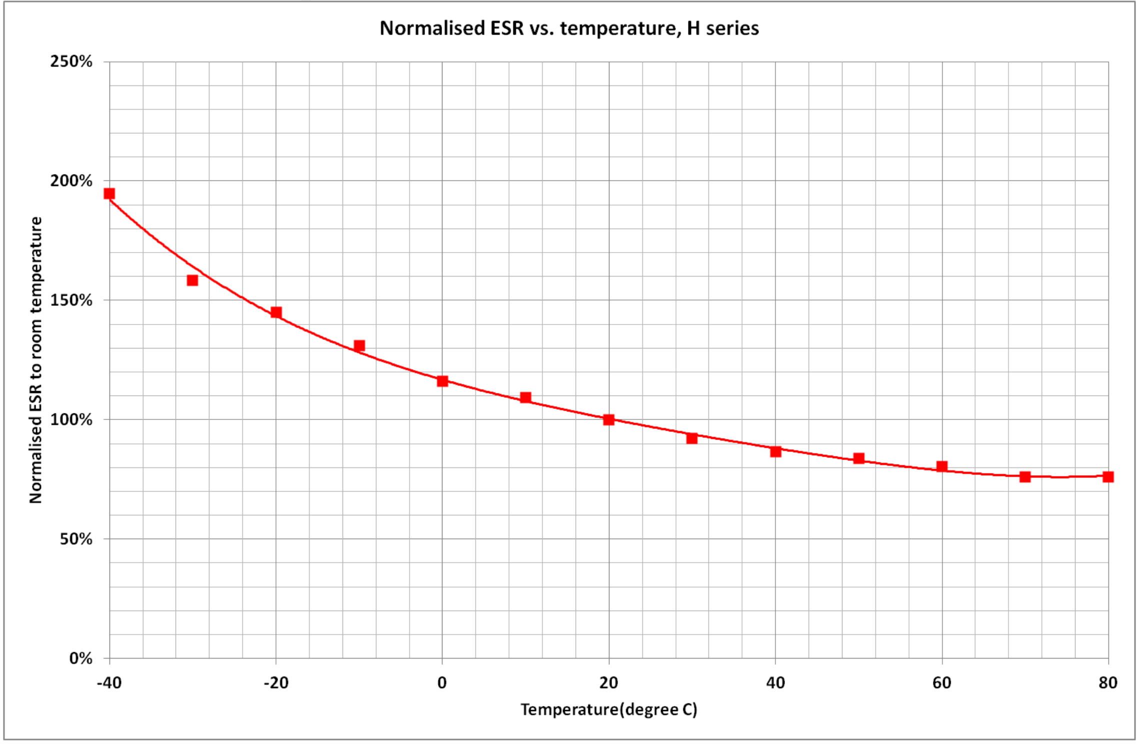

Figure 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~1.9 x ESR at room temp, and that ESR at 70ºC is ~0.8 x ESR at room temperature.

Frequency Response

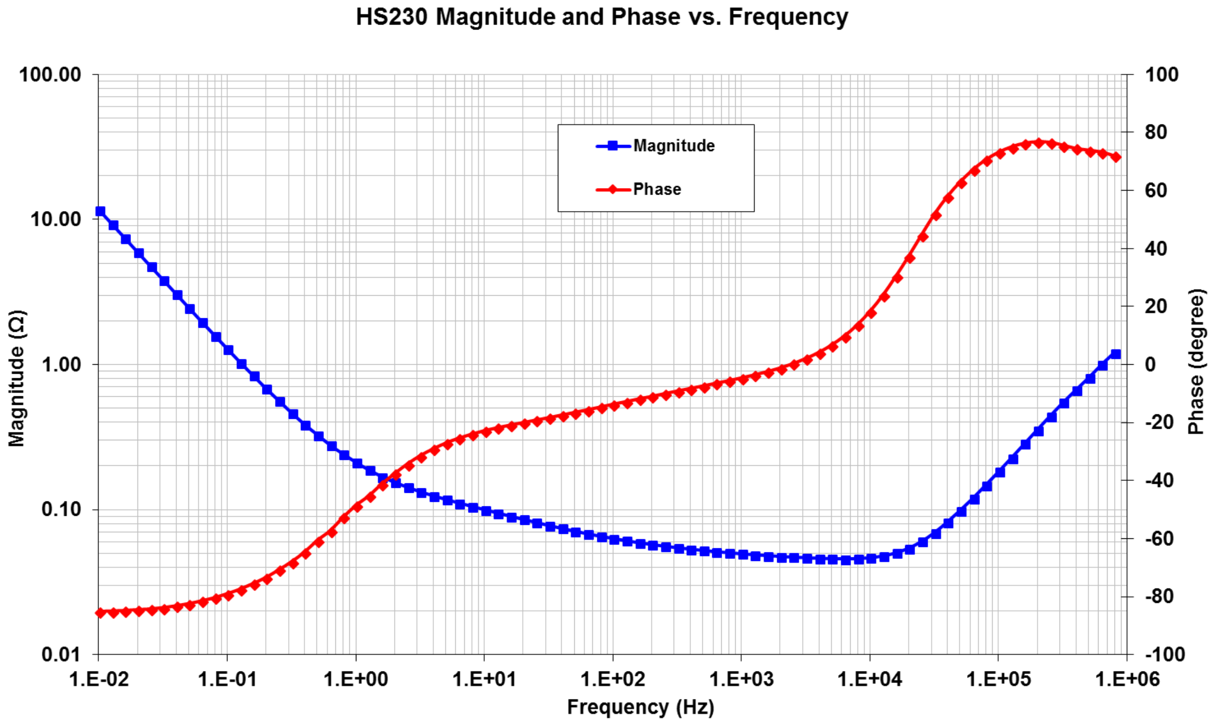

Fig 8: Frequency Response of Impedance (biased at 5.5V with a 50mV test signal)

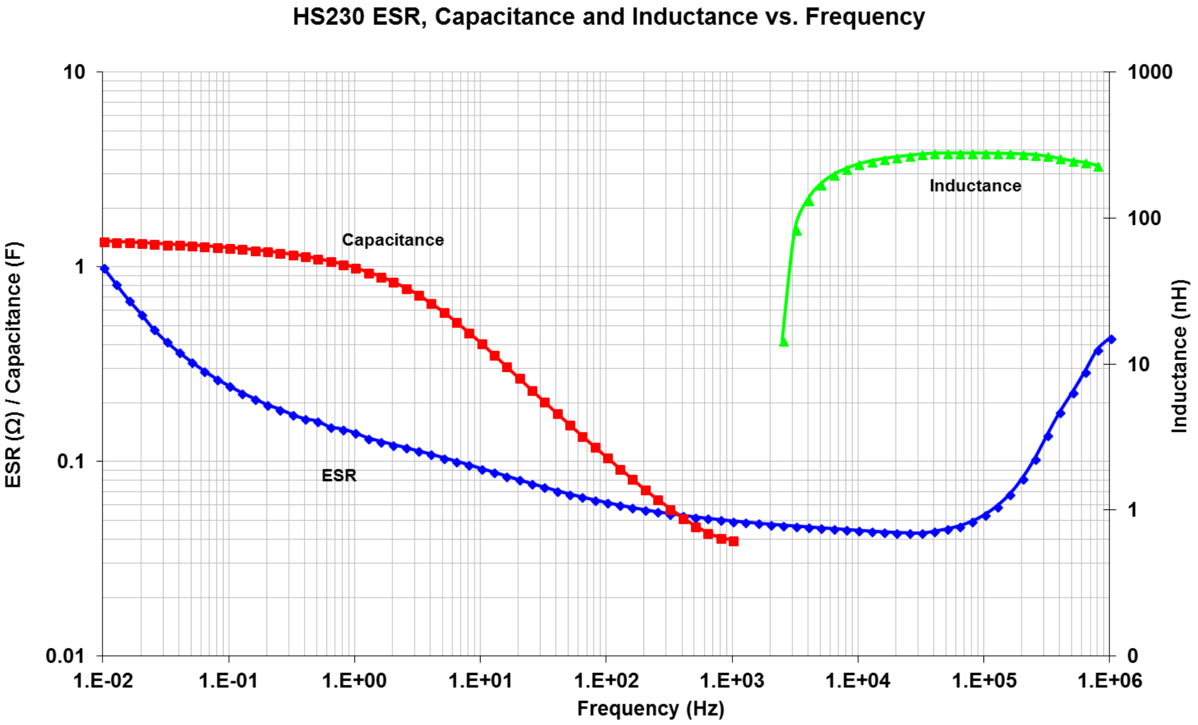

Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx 1 Hz when the magnitude no longer rolls off proportionally to 1/freq and the phase crosses -45°. Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulsewidth.

Leakage Current

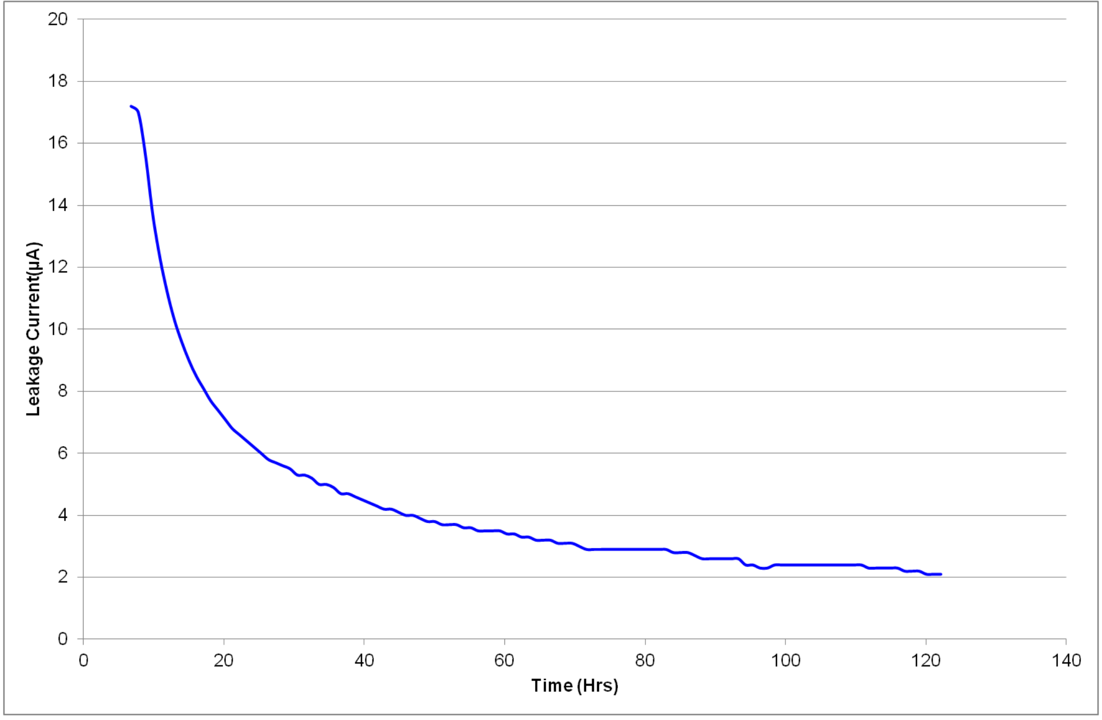

Fig 10: Leakage Current

Fig 10 shows the leakage current for HS130 at room temperature. The leakage current decays over time and the equilibrium value leakage current will be reached after ~80hrs at room temperature. The typical equilibrium leakage current is 3µA at room temperature. At 70°C leakage current will be ~10µA.

Charge Current

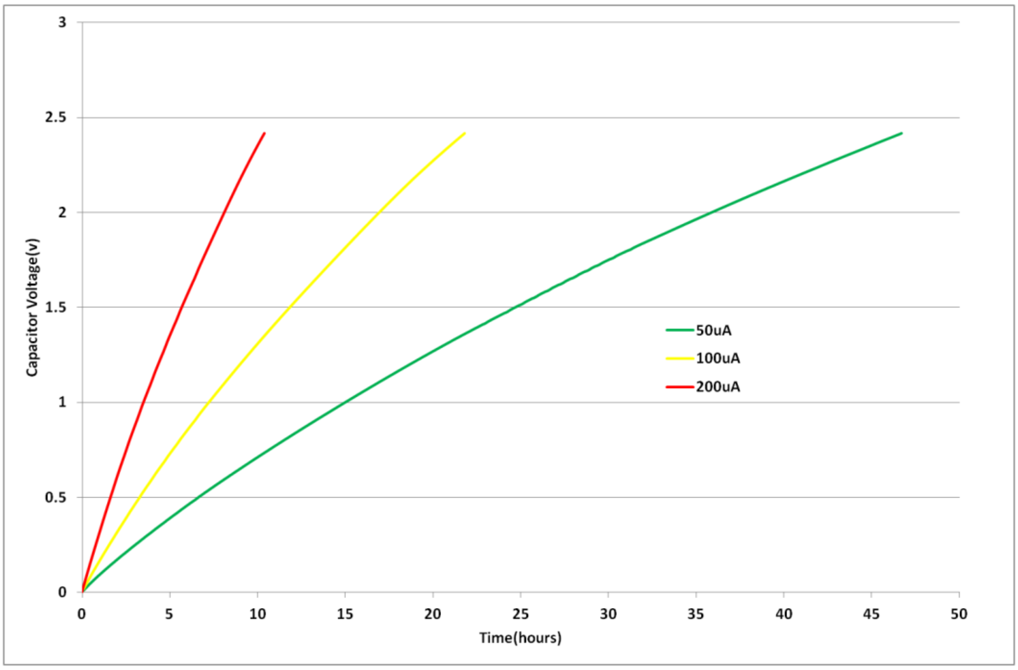

Fig 11: Charging an HS130 with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take 2.4F x 2.4V / 0.00005A = 32hrs to charge a 2.4F supercapacitor to 2.3V at 50µA, but Fig 11 shows it took 47hrs. At 200µA charging occurs at a rate close to the theoretical rate.

RMS Current

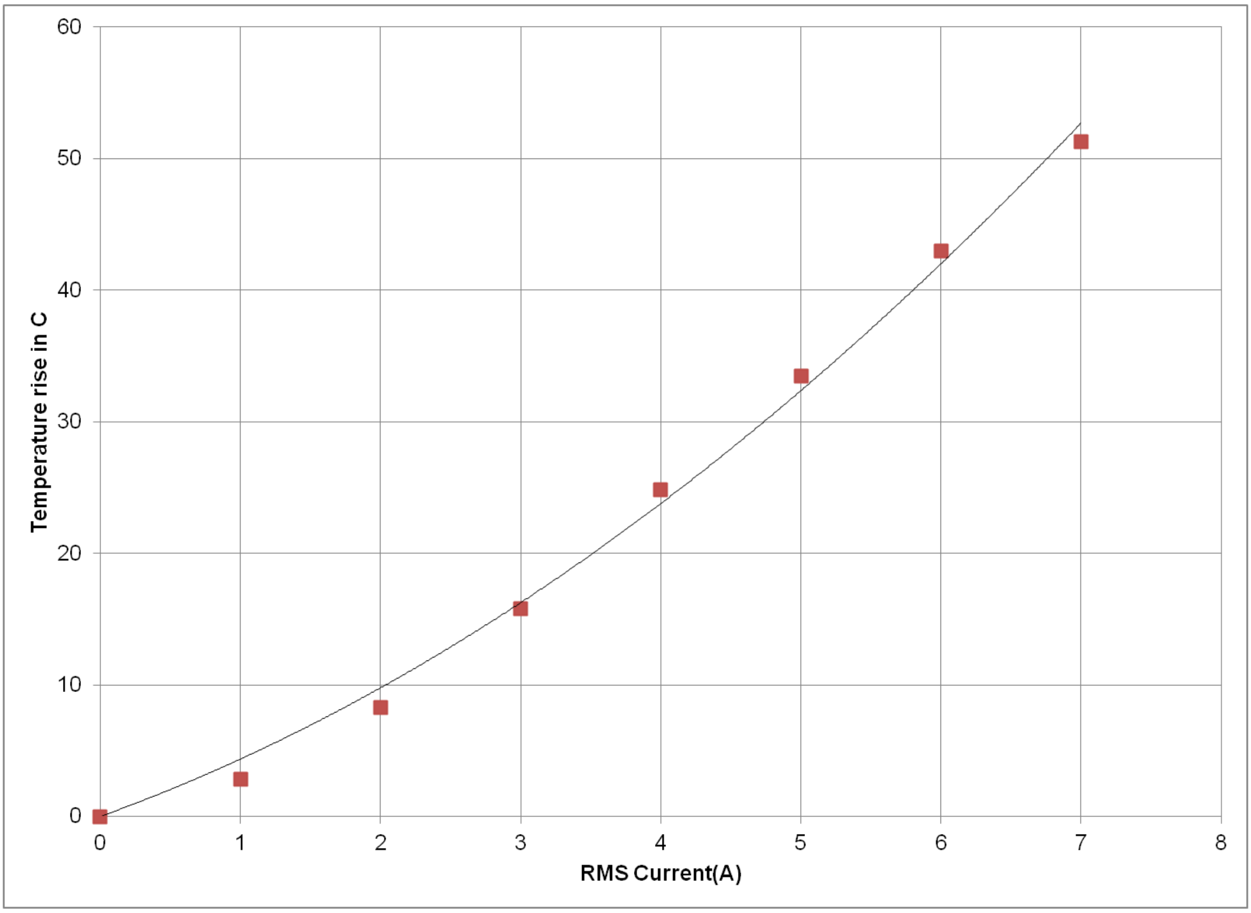

Fig 12: Temperature rise in HS230 with RMS current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, and then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 70°C, then the maximum RMS current should be limited to 4.75A, which causes a 30°C temperature increase.

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